

Advanced DSP Architectures using ANSI Standard Interconnects; FPDP, Serial FPDP, Raceway, and Fibre Channel

Today's advanced Digital Signal Processing (DSP) Systems must handle very high data rates in an efficient and cost effective manner. System architectures for data acquisition, data movement, data processing, and data storage have evolved from specially designed, proprietary interconnects to the use of industry standards. There now exists a rich set of ANSI standard interconnect technologies that allow the integration of cost effective, high bandwidth, advanced DSP systems. This paper presents a typical architecture for advanced DSP systems and provides a technical overview of four standard interconnect technologies to include: RACEway, FPDP, Serial FPDP, and Fibre Channel. It then provides specific examples of how these standards technologies can be deployed in systems to fulfill the cost effective, high throughput, interconnect requirements of advanced radar, sonar, medical and other DSP applications.

TYPICAL DSP SYSTEM ARCHITECTURE

There are four primary subsystems that make up the modern advanced DSP system as shown in figure 1. The sensor subsystem scans its environment, performs high-speed analog to digital (A/D) conversions, and outputs continuous streams of high-speed digital data. The DSP subsystem, generally a cluster of interconnected DSP's, processes these data streams and outputs high bandwidth usable image data. Then General-Purpose Computers (GPC) display, store, and/or further analyze these images. And critical to most DSP systems at selected points along the data path are high-speed storage (data recorder) subsystems that provide data recording, playback, and direct workstation access. The interconnects between these primary DSP system elements must be chosen

according to the throughput, latency, distance, noise immunity, cabling characteristics, and cost constraints of the program.

ANSI STANDARDS ORGANIZATIONS

The RACEway Interconnect, FPDP, and proposed Serial FPDP standards are being developed and maintained under the VITA Standards Organization (VSO). VITA (VME Industry Trade Association) was accredited as an ANSI (American National Standards Institute) standards development organization in June of 1993. The VSO has been instrumental in the development of 17 approved ANSI standards and currently has over 15 more standards in task groups under development. Many of these standards have been extremely valuable to the growth and development of the embedded systems market. Complete information on these stan-

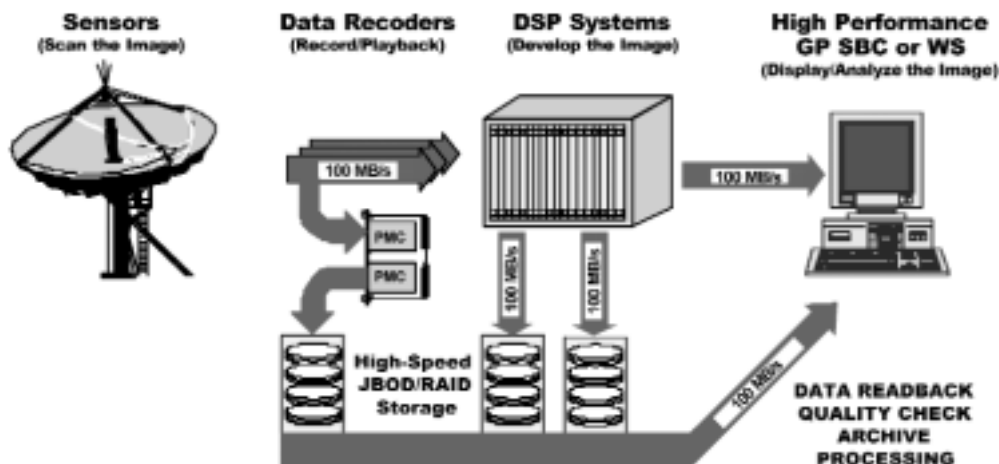


Figure 1. Advanced DSP System Architecture.

ards is available at the www.vita.com web site. The Fibre Channel standard was developed by the T11 Technical Committee under the National Committee for Information Technology Standards (NCITS); also an ANSI accredited standards development body. Additional information on TC T11 and NCITS can be found at the www.ncits.org and www.t11.org web sites, respectively.

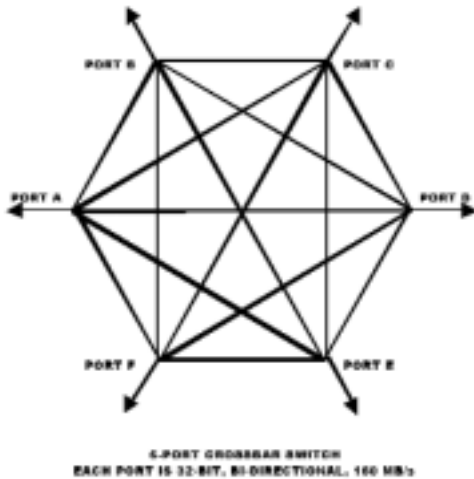


Figure 2. RACEway Crossbar Switch.

RACEWAY INTERLINK

The ANSI/VITA 5-1994 RACEway Interlink, developed by Mercury Computer Systems, Chelmsford, MA, has gained acceptance from DSP board suppliers as a high-speed interconnect between DSP boards. RACEway was specifically designed to be a high-speed, switched-fabric interconnect between multiple high bandwidth processing elements all sharing the same backplane within a single VME chassis. RACEway is a switched fabric for 32-bit parallel data paths. One or more cascaded 6-port crossbar switches (figure 2) on the backplane implement point to point connections between end points on demand. Each point to point connection, once established, operates at 160 MB/s. Simultaneous communications between end points is supported. Thus a 6-port crossbar can support three simultaneous point-to-point connections and an aggregate burst rate throughput of 480 MB/s. Over fifteen companies provide an array of I/O and data storage products for RACEway based DSP systems. This will continue well into the future as new RACE++ extensions will increase the speed of each link to 266 MB/s and increase the size of each crossbar from 6 to 8 nodes. The standardization work for RACE++ is being done under the VITA 5.1 Task Group.

FPDP

FPDP (Front Panel Data Port) initially evolved as a defacto standard for the sensor-to- DSP interconnect, but has recently been approved as an ANSI standard (ANSI/VITA 17-1999). It is available in products from over twenty sensor and DSP companies, and its adoption rate into new sensor and DSP products is growing rapidly. FPDP connects across the front panel of VME

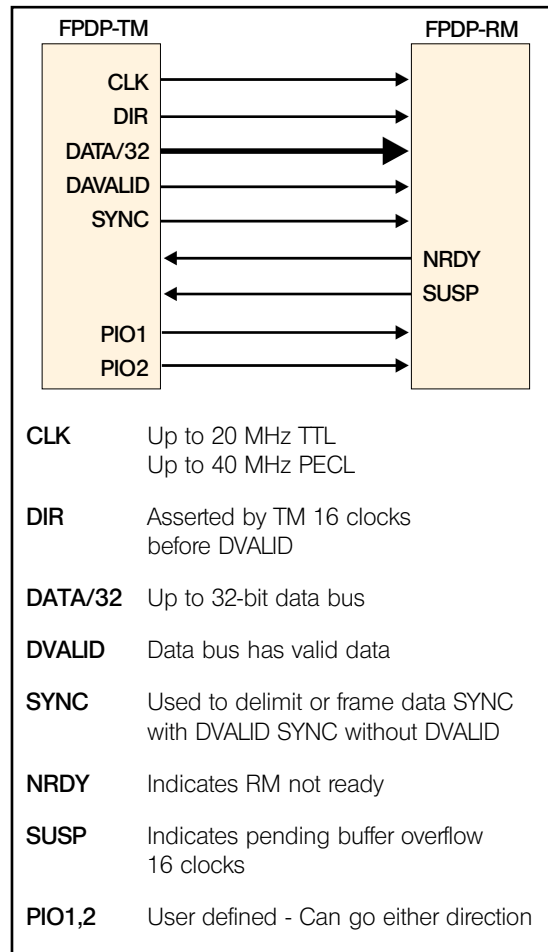


Figure 3. FPDP Signals.

boards using a inexpensive ribbon cable. The data flows across a 32-bit parallel, synchronous interface from FPDP Transmitter to one or more FPDP Receivers. There is no addressing as the interface is specifically

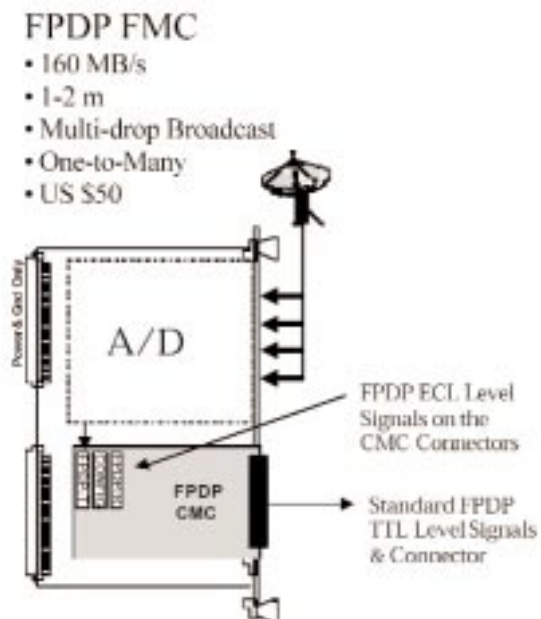


Figure 4. FPDP FMC.

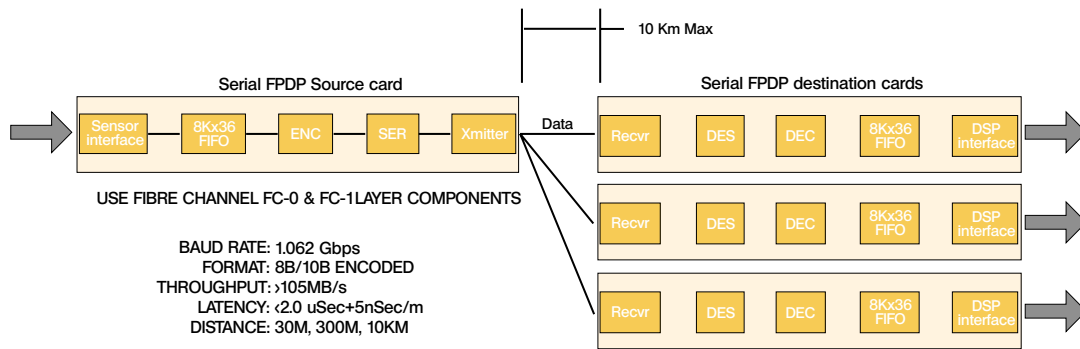


Figure 5. The Serial FPDP Concept.

intended to handle continuous streaming data from the A/D converter of a sensor. There is also no contention since only one transmitter is permitted to be active on the bus. Control of multiple transmitters can be done external to the FPDP, but is not a part of the standard. The FPDP interface design is both simple and fast with a maximum data throughput of 160 MB/s. FPDP also includes a SYNC signal to delimit frames of data and a SUSPEND signal provides flow control, if desired. Two bi-directional signals, PIO1 and PIO2 are available for user defined functions. Figure 3 lists all of the FPDP signals and describes their functions. FPDP provides a simple, high-bandwidth, and reliable sensor-to- DSP connection.

FPDP Implementation

In order to provide flexibility in the sensor interface a concept has been developed which utilizes another standard, the Common Mezzanine Card (CMC). By putting the standard FPDP signals on the connectors of a CMC form factor, circuitry on the mezzanine provides the means to reformat the FPDP data to other standard interfaces such as Serial FPDP and Fibre Channel to be discussed later. Following the naming convention of PCI + CMC = PMC, then FPDP + CMC = FMC. The FPDP FMC card shown in figure 4 is a very simple card that converts the ECL level FPDP signals on the FMC motherboard connectors to TTL level signals and face plate connector as specified by the FPDP standard. Recently, an association of FPDP Partners has been formed to promote the use of FPDP. In addition, the group has begun work to develop the specification for FPDP2 that could increase bandwidth to over 400 MB/s. More information on FPDP and its future can be found at the www.fdpd.com web site.

SERIAL FPDP

In some applications, the distance between the Sensor and DSP is beyond the reach of the FPDP parallel cable. Serial FPDP is a new technology developed by Systran Corporation, Dayton, Ohio specifically to address the need for distance between the sensor and DSP beyond the one-meter cable limitation of the parallel FPDP. Serial FPDP was designed to be a transparent extension of FPDP to distances up to 10 kilometers. The basic concept, shown in figure 5, is relatively simple. Input standard FPDP data, encode, serialize, and transmit the FPDP data and control signals

over a gigabit serial link. At the other end, receive, deserialize, and decode the information back to standard FPDP data output. The ENDEC (encoder/decoder), SERDES (serializer/deserializer), transceivers, and cabling (optical or copper) are all borrowed from standard Fibre Channel technology. These components, operating at a gigabit per second, are well tested and readily available. The Serial FPDP link has a maximum throughput of over 105 MB/s and a latency of about two microseconds plus 5 nanoseconds per meter of cable. A simple crossbar switch is available which can switch and/or replicate an input signal to as many as 32 output ports. This simple broadcast capability is very useful in some applications.

Serial FPDP Implementation

Following the concept of FMC flexibility for the sensor interface, figure 6 shows a Serial FMC interface that is available to convert the FPDP output of the sensor to either optical or copper Serial FPDP format. Also shown in figure 6 is a 32-port crossbar matrix switch (NTS). Any of the 32 input ports can be directed to one or more output ports. It is a static switch controlled via RS-232. Modular port cards allow both port expansion and media conversion. Serial FPDP technology has been proposed to the VITA organization as a companion standard to the ANSI Standard FPDP. The standardization work is being done under the VITA 17.1 Task

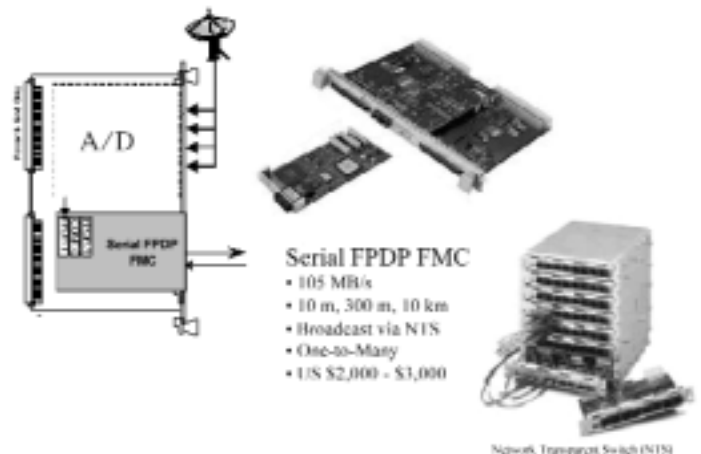
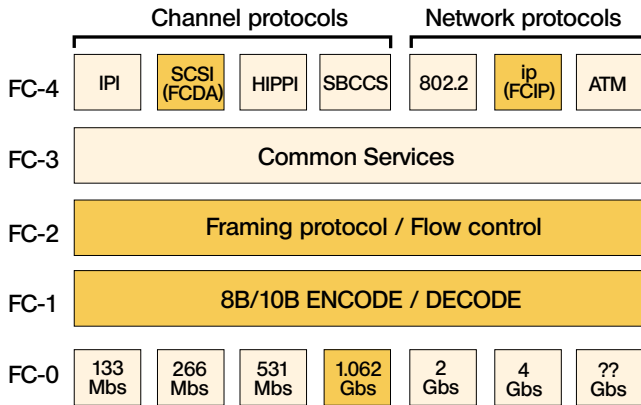


Figure 6. Serial FPDP FMC & Crossbar Matrix Switch



Optical: Shortwave Laser, Longwave Laser
Copper: Twinax, Coax, Others

Figure 7. Fibre Channel Layers.

Group.

FIBRE CHANNEL

Technical Committee, T11, was formed in 1988 to develop an ultra high-speed transport which would fulfill the requirements of next generation mass storage, peripheral I/O, and networking. It was developed from the ground up to be a universal carrier of data and upper layer protocols, both channel (e.g. SCSI) and networking (e.g. IP). The technology was called Fibre Channel. Fibre Channel is an extremely robust and flexible technology; therefore, it can be extremely complex and confusing on its many layers. There are literally hundreds of specifications, documents, technical reports, and books that describe all the options within the five layers of Fibre Channel, shown in figure 7. Fortunately, the Fibre Channel technology and the market have matured to the point where most of the common options and complexity are contained within readily available Fibre Channel ASIC's, Host Bus Adapters, drivers, backplanes, hubs and switches. The FC-0 layer defines the physical layer of Fibre Channel. Commonly used options at this layer include a serial baud rate of 1.063 Gigabits/s. The twinax copper cable will have either the DB-9 or the HSSDC connector and

the optical 50/125 micron, multimode cable will generally be equipped with the dual SC connector. The FC-1 layer defines the 8B/10B encoding, ordered sets, framing, and other primitives used to control and maintain proper link functions. This layer is well defined and implemented in virtually all the FC ENDEC's and ASIC's. The FC-2 layer is the signaling and framing protocol layer. It specifies addressing, sequence management, three different topologies, and three classes of service. The most common topology has been the Fibre Channel Arbitrated Loop (FC-AL). The point-to-point topology is rarely implemented; however, the switched fabric topology is maturing and will become an important factor in the future. The circuit switched Class 1 is obsolete and Class 2 is also rarely implemented.

Class 3 is the most common class of service in use today. It is a connection oriented class of service with flow control, but without the data acknowledge of Class2. Class 3 is well suited to upper layer protocols such as SCSI and TCP/IP that verify data delivery and handle error and retry requirements at the driver level. The FC-3 layer was intended to define a set of common services to the FC-4 layer above. However, no standards have ever been completed at this layer. The FC-4 layer defines the Upper Layer Protocols (ULP) which can be carried by Fibre Channel. There are many options defined; however, the SCSI Fibre Channel Protocol (SCSI FCP), initially defined for mass storage and later also used for peer-to-peer communications, has dominated. The TCP/IP (FC-IP) and Virtual Interface Architecture (FC-VI) profiles are likely to become important as they become better defined and the Fibre Channel commercial markets mature.



Figure 9. Storage Area Network (SAN) Switch.

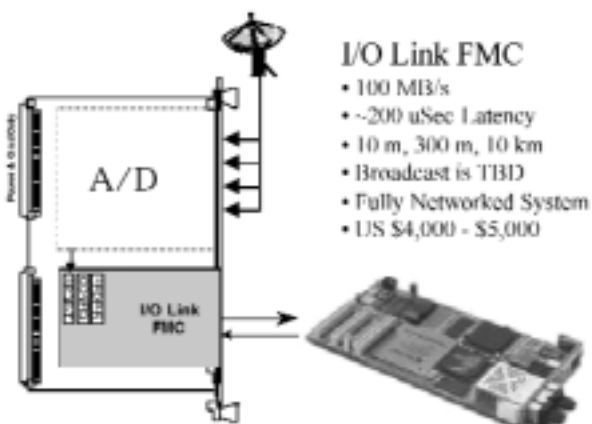


Figure 8. I/O Link FMC.

Fibre Channel Implementation

Again following the concept of FMC flexibility for the sensor interface, figure 8 shows the I/O Link FMC. The circuitry of the I/O Link FMC makes the streaming FPDP sensor data available to the Fibre Channel network. The I/O Link uses the same SCSI Fibre Channel Protocol as disk drives; thus, the sensor interface has a behavior similar to disk drives on the network. This allows other devices on the network to read and write data to and from the sensor as well as control and monitor sensor operating parameters and status. Fibre Channel Fabric Switches have been available for many years. However, these fabric switches are complex devices designed for very large enterprise networks with hundreds or even thousands of nodes. This com-

INTERCONNECTS

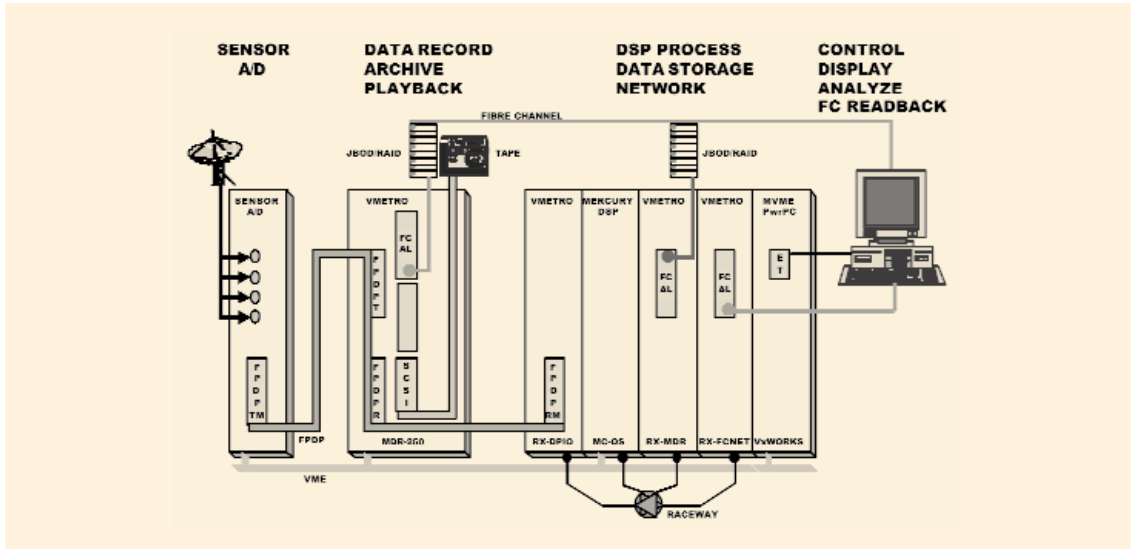


Figure 10. DSP with FPDP, RACEway, & Fibre Channel.

plexity imposes a heavy burden on the suppliers of Host Bus Adaptors (HBA) in the form of complex driver software that must handle the special login processes and name server handling procedures required to operate in a fabric switched environment. As a result, the far simpler FC-AL topology has dominated the smaller systems found in the storage and embedded systems market. Now, the recent introduction of the Storage Area Network (SAN) Switch (figure 9) will dramatically change the way Fibre Channel is implemented in future DSP systems. The SAN switch is designed to drop seamlessly into the FC-AL environment and transparently convert multiple "share the bandwidth" loops into a fully switched architecture. The SAN switch looks at the 8-bit loop address of each incoming FC frame and routes it directly to the appropriate output port. Thus communicating devices are provided with what appear to be dedicated 100MB/s links. Connections are dynamic and the SAN switch supports non-blocking, simultaneous communications between ports. The SAN switch increases the aggregate throughput of the system from a fixed 100MB/s to

a maximum of $(n/2) \times 100\text{MB/s}$ where n is the number of non-blocking switch ports. The Fibre Channel technology is an excellent fit for today's distributed DSP systems. It is one of the highest bandwidth networking solutions, with products available today, achieving 100 MB/s of sustained throughput. It has also been accepted in the commercial market as the next generation technology for mass storage and storage area networks. This provides the product volumes required to realize the COTS goals of reduced pricing and product longevity. Fibre Channel development continues in the TC T11 committees today. Fibre Channel products that operate at 2 Gbits/s have been announced and switches that deliver the speed and connectivity required for tomorrow's embedded DSP systems are emerging today.

DSP ARCHITECTURES USING STANDARDS

Figure 10 is an example of a complete DSP system designed using RACEway, FPDP, and Fibre Channel ANSI standard interconnects. The FPDP provides the

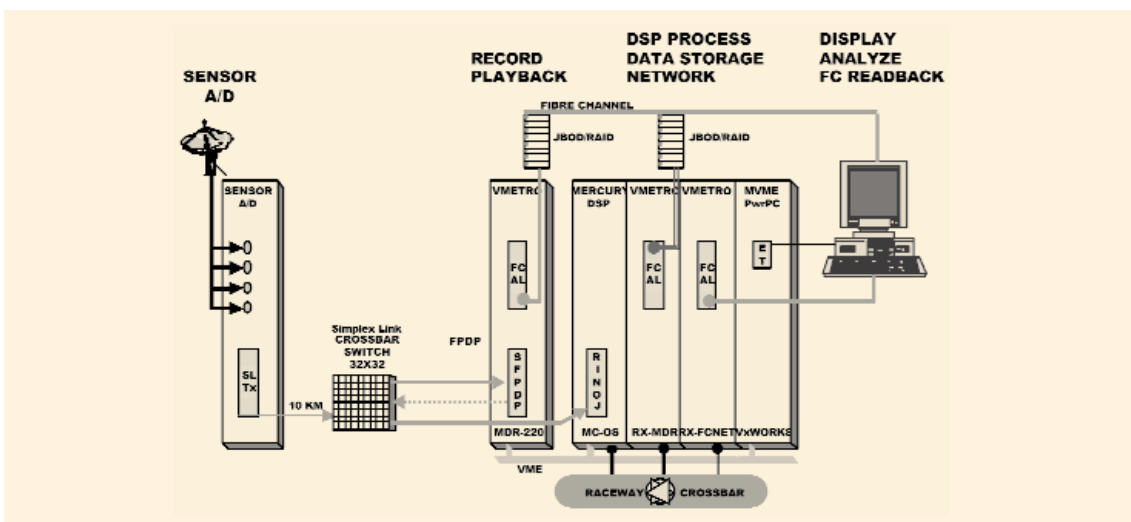


Figure 11. DSP System with Serial FPDP.

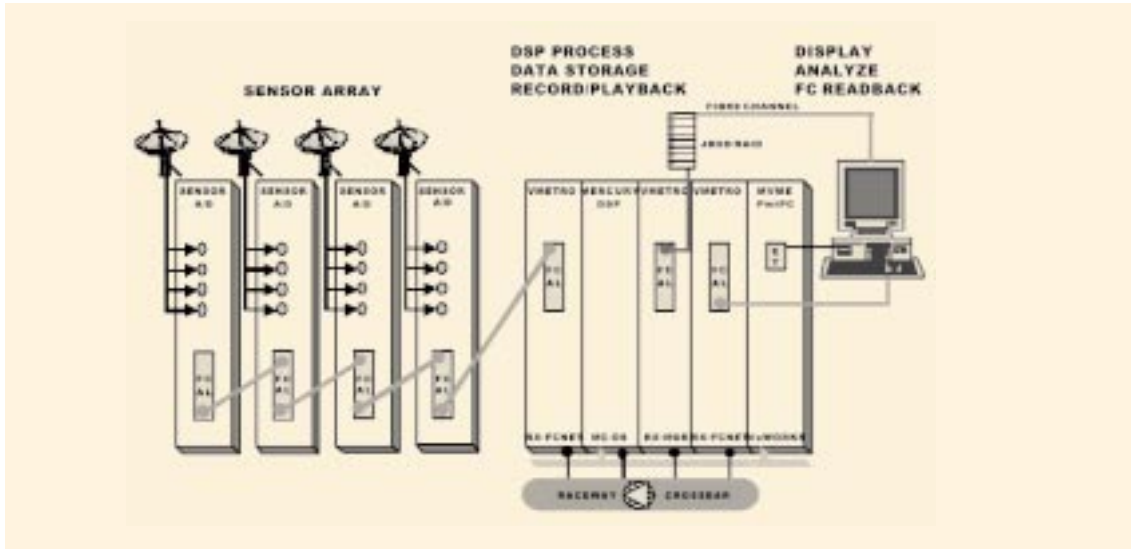


Figure 12. DSP with Fibre Channel Arbitrated Loop (FC-AL).

multi-drop connection from the sensor to a raw data record/archive/playback device and also the input to the DSP system. In this example the recorder is a VMETRO MIDAS Data Recorder (MDR-250) and the input to the DSP is a VMETRO RACEway Digital Parallel I/O (RX-DPIO) board. The data recorder has both an FPDP receive and transmit interface. During data acquisition the receive interface is used to passively record all of the raw sensor data as it is fed into the DSP. Later, the transmit port is used to playback the recorded data, effectively simulating real-time sensor data input to the DSP. The recorder utilizes a dedicated high-speed FC-AL link to stripe the data across a Fibre Channel equipped JBOD (Just a Bunch Of Disks) or RAID (Redundant Array of Independent Disks) at speeds approaching 100MB/s. A second FC-AL port on the disks provides the workstation with direct high-speed access to the recorded data. The recorder also includes a standard SCSI interface for post-run data archiving to a high-speed, high-capacity tape drive. The I/O and processing within the DSP computer is based on the ANSI standard RACEway. The FPDP to

RACEway I/O Controller (RX-DPIO) distributes the sensor data from FPDP to the DSP processing elements via the RACEway. A RACEway to Fibre Channel recorder interface (RX-MDR) provides the path to/from Fibre Channel storage similar to the external FPDP data recorder. The RX-MDR interface allows data to be recorded to disk at any point along the processing path. Again, the workstation also has direct access to the Fibre Channel disks for post-run analysis or archive of the processed data. Another RACEway to Fibre Channel I/O Controller (RX-FCNET) provides a high-speed, real-time networking capability to one or more general-purpose workstations for display and further analysis of the processed data. Figure 11 shows a similar DSP system architecture that includes the Serial FPDP technology for the sensor-to-DSP connection. This allows the system components to be highly distributed up to 10 kilometers apart. A Serial FPDP cross-bar switch is employed to replicate and retransmit the Serial FPDP data simultaneously to both the recorder (MDR-220) and the DSP processing system. In fact, the switch could replicate the signal to 32 devices, and if

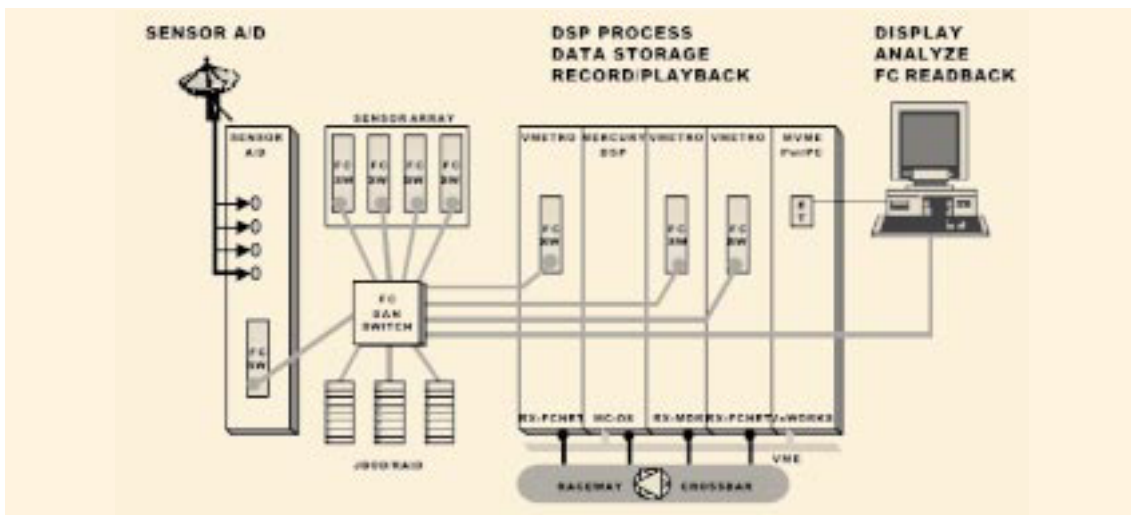


Figure 13. Switched Fibre Channel DSP System in Y2000.

multiple switches are cascaded, the signal could be transmitted to literally thousands of destination devices simultaneously. The crossbar switch can also switch its input from the sensor to the recorder, for playback of the recorded data into those same thousands of destination devices. Figure 12 shows a DSP architecture that utilizes the I/O Link FMC in the sensor to connection multiple sensors to the DSP via the FC-AL. FPDP and Serial FPDP are excellent choices to connect a single high bandwidth sensor to one or more destinations, however these interfaces cannot network an array of low bandwidth sensors into a single input data stream to the DSP system. This is one of the primary advantages of the FC-AL. Because the FC-AL cannot broadcast or replicate its data to multiple receivers at the same time, the raw data recording and playback function must be done using the RX-MDR within the RACEway environment. Figure 13 shown an advanced DSP design made possible by a new device, the Storage Area Network (SAN) Switch. The SAN switch allows all Fibre Channel devices; sensors, disks, DSP, and workstations, to be connected via switched fabric without the complexity of the full up Fibre Channel Fabric Switch. Control, data, and status from any device to any device over dynamic, dedicated, 100MB/s connections are possible in the SAN switched system. The switched DSP system can be easily expanded as requirements evolve or change by simply adding sensor, storage, DSP, or workstation resources as necessary to the switched environment. The fully networked system provides the high-bandwidth, connectivity and scalability required from DSP systems today and tomorrow.

SUMMARY

ANSI standard interconnect technologies developed by the VITA and NCITS provide the tools for building COTS based, advanced DSP systems. Industry use of these standards allows the system developers to integrate multi-vendor systems using a variety of components that best meet the operational needs and cost objectives of each individual program ■

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