

VIM Mezzanine Boosts VME Bandwidth

Few mezzanine designs have evolved into true industry standards. Unfortunately, the most popular standard mezzanine busses still fall far short of meeting the needs of recently-introduced DSP and RISC processors. In trying to close this I/O gap, Pentek has developed the VIM (Velocity Interface Mezzanine) architecture, a new, high-performance mezzanine bus delivering extremely high-speed data transfers suitable for a variety of processors and board formats.

INTRODUCTION

Embedded system design will always be challenged to match the performance levels of latest technology components. With memory density, CPU horsepower and data rates doubling every few moments, the roles of the interconnect structures of standard open-architecture busses and boards are being redefined and new techniques of moving data are evolving.

Over the years, mezzanine boards have proven themselves as excellent solutions for connecting high-speed peripherals to VMEbus boards. They offer a win-win approach because they remove data traffic from the backplane, deliver higher sustained rates over a dedicated channel, and yield a very modular approach to system design.

Many of these mezzanines were developed by individual vendors for a specific purpose and were, therefore, destined to remain as custom, proprietary designs. However, a few gained acceptance from several vendors and were propelled by industry groups towards standardization. An excellent example is the PMC (PCI Mezzanine Card), currently found on over half of all VMEbus single board computers.

Nevertheless, none of the existing popular mezzanine standards today, including PMC with its 132 MB/sec PCI bus, can match the data transfer demands of the new crop of high-speed DSP and RISC processors already on the market.

DEFINING A NEW MEZZANINE

In 1997, our design engineers were tasked with selecting a mezzanine to supply high-speed I/O to our new quad DSP processor board based on the TMS320C6201. We needed to be able to deliver data to these processors at a rate comparable to the synchronous data bus speed of the DSP, which meant 400 or 800 Mbytes/sec, depending on the mode. We also had to eliminate bottlenecks by ensuring that each processor had its own private,

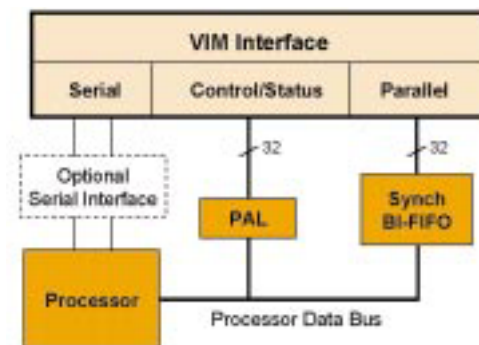


Figure 1. Three sections of the VIM Interface.

dedicated path.

Ideally, we needed a 32-bit bus with a 100 MHz clock, to provide the minimum 400 MB/sec rate required. With this bandwidth, each DSP could take advantage of the many data interfaces we had targeted for the processor board including FPDP (front panel data port), RACEway, and wideband A/D converters.

Of vital importance, the mezzanine needed to be processor independent and either already an industry standard or capable of becoming one. The mezzanine had to be robust and low-cost while providing ample

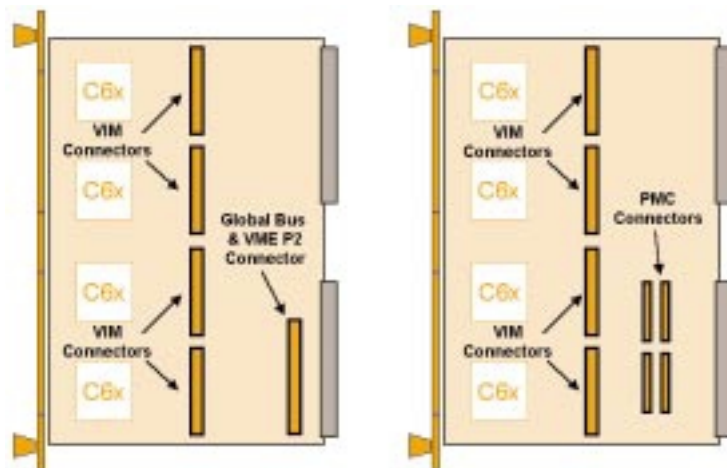


Figure 2a. Connector location - 4290/91 (left side)

Figure 2b. Connector location - 4292 (right side)

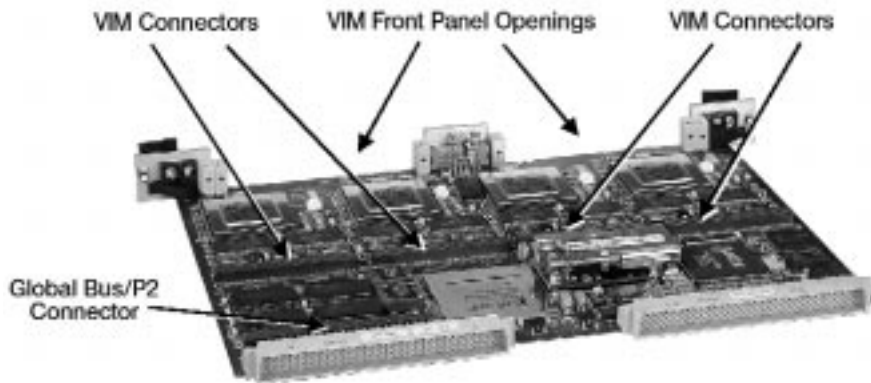


Figure 3. Quad C6x DSP VIM Baseboard.

room for a reasonable amount of circuitry along with its associated cooling and shielding. Access to the front panel was essential so that specialized connectors could be incorporated to meet many different types of analog and digital signals.

Another requirement of the new mezzanine was provision for a high speed synchronous serial interface, commonly found on many of the new processors aimed at digital telecom applications. Lastly, the processor needed a means for controlling functions and monitoring status of the mezzanine circuitry.

Altogether, these requirements outstripped the performance levels of all existing mezzanines, which led us to defining a new mezzanine standard.

OVERVIEW OF VIM - VELOCITY INTERFACE MEZZANINE

After selecting the name VIM, for Velocity Interface Mezzanine, many conflicting factors influenced its design. We started the specification with one eye clearly focused on roadmaps for future processors so that VIM would not only accommodate future TI processors, but other DSP and RISC processors as well. We also realized the importance of the PMC module specifica-

tion and wanted to make mechanical decisions which would allow the "peaceful coexistence" of PMC modules when they were appropriate. Lastly, we were under some significant deadline pressure to get our new product to market!

The three basic elements of the VIM electrical interface are shown in figure 1 and consist of a high speed streaming parallel interface, a synchronous serial interface and a control/status interface.

VIM Streaming Parallel Interface

From the beginning, we realized that in order to define an open-architecture specification, the high-speed streaming parallel interface must not be locked to the timing of any particular processor. The best solution proved to be installing a synchronous bi-directional FIFO memory between the processor and the VIM interface. Since these Bi-FIFOs follow industry-standard timing, several vendors provide compatible products in various speed and density versions. Many processors already include a glueless hardware interface for synchronous DRAMs, quite similar to the timing required for synchronous Bi-FIFOs.

As it turns out, these synch Bi-FIFO's not only solve the timing problem, they are also ideal for buffering data

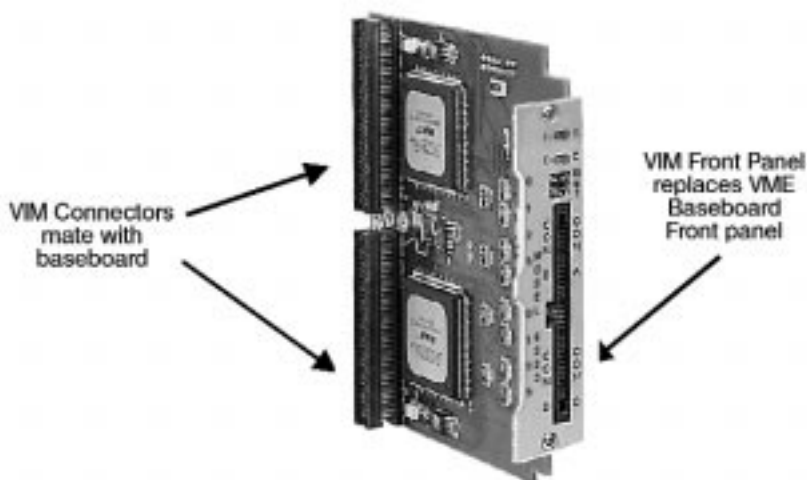


Figure 4. Typical VIM-2 Module.

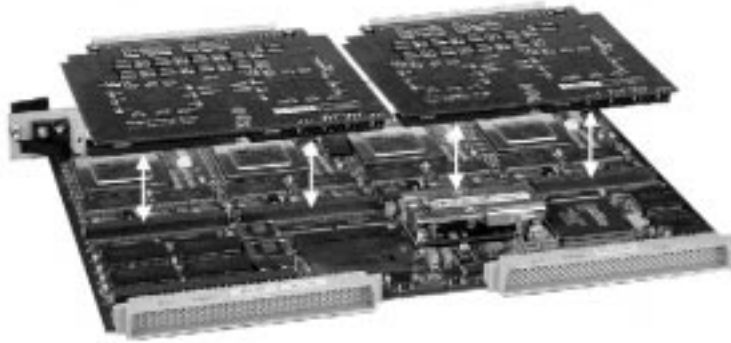


Figure 5. Attaching 2 VIM-2 modules to VIM Baseboard.

blocks to and from the processor. Processors usually have programmable DMA controllers which can dramatically improve processor efficiency by offloading the tasks of moving data. These DMA controllers can be started automatically by external interrupts connected to the programmable Bi-FIFO status flags to generate an interrupt whenever the data within the Bi-FIFO reaches a specific level. In this way, every time the Bi-FIFO needs servicing, data is transferred to and from internal processor memory with no CPU intervention required.

Bi-FIFO's nicely accommodate both fast and slow external interfaces on the mezzanine side, effectively isolating the processor from these transfer details. External data can be staged in the Bi-FIFO and then efficiently moved in fast bursts to the processor using the DMA controller. The processor no longer needs to play the role of "I/O baby sitter", holding up execution waiting to send or receive data to the interface.

Not all processors are capable of sustaining the high data rates required by some of the new interface standards. The new RACE++ standard sends packets of 32-bit data words at a transfer rate of 66.66 MHz. Fortunately, the Bi-FIFOs act as an elastic store to capture incoming data packets at the full rate, allowing the processor to subsequently read out the packet words at a much lower rate. Likewise, outgoing packets can be composed at a modest rate. Once completed, they can "burst" out of the Bi-FIFO at the full word rate of the interface.

VIM Serial Interface

VIM supports two synchronous serial ports with bit rates up to 100 MHz. Each full-duplex port contains two data lines, three clock lines and two framing lines. This arrangement is consistent with many serial interface devices including E1 and T1 digital telecom framers, audio codecs, modems, data acquisition subsystems and many types of microprocessors.

As an example, Texas Instruments new 'C6203 processor is capable of handling a full T1 span of V.90 modems and the VIM serial port makes an ideal connection to a T1 line interface mezzanine.

VIM Random Access Control/Status Interface

Since every mezzanine board has circuitry on board

which may need to be configured and monitored, the VIM specification includes a read/write address space into which mezzanine registers and other devices can be memory mapped. In this way, to control a function, the processor simply accesses a unique location and performs a read or write operation. The data bus is 32 bits and the address bus is 16 bits, more than enough to handle even the most complex peripheral chips.

Power Supply

Rounding out the electrical connections are the power supply lines which provide ground, +5v, +12V and -12V supplies. A total maximum power dissipation of 15 watts is recommended.

MECHANICAL ASPECTS OF VIM

VIM Connector

Pin-and-socket style connectors were chosen to join the mezzanine to the processor board because of their high density and excellent reputation for reliability. These 4-row, 160-contact connectors occupy merely 0.5 square inches of real estate and are available in both male and female versions, with surface mount pads to preserve routing space on inner PCB layers.

Quad Processor VIM Baseboards

The first VIM baseboard was the Model 4290 Quad

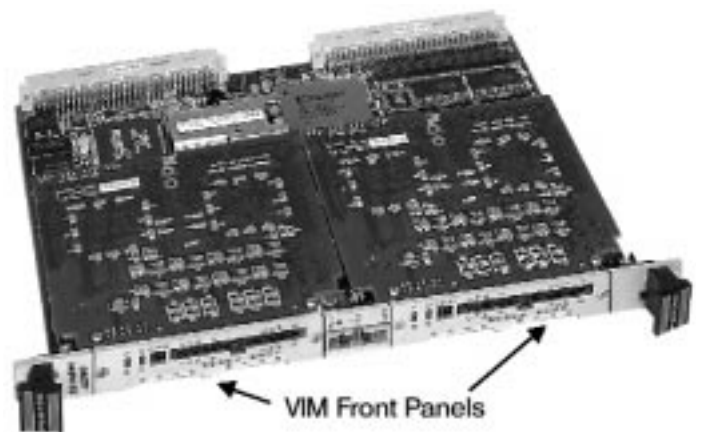


Figure 6. Two VIM-2 Modules nested in same slot as VIM Baseboard.

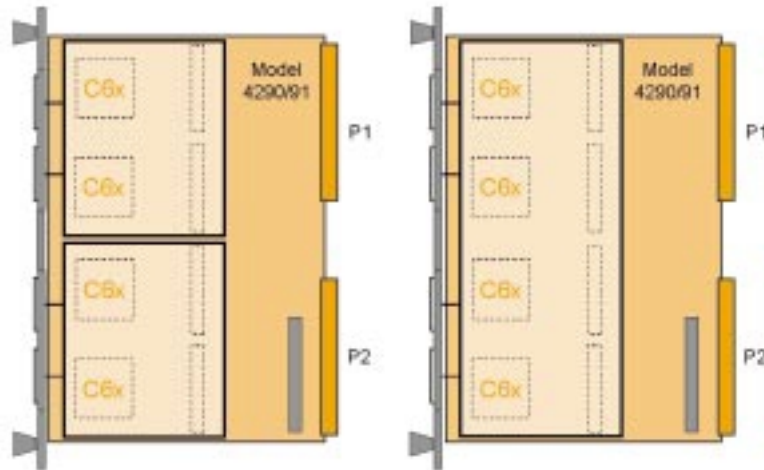


Figure 7 (left side). Two VIM-2 Modules.
Figure 8 (right side). VIM-4 Module.

'C6201 DSP Processor. This was soon followed by the Model 4291 Quad 'C6701 DSP and then most recently, by the Model 4292 Quad 'C6203 DSP. All are standard 6U VMEbus boards featuring four VIM connectors for simultaneous, high-bandwidth I/O connections to all four processors.

Figures 2a and 2b show the placement of the four VIM connectors for both the Model 4290 and 4291 and the Model 4292, respectively. Note that the 4290 and 4291 include a fifth connector which provides access to the global data bus as well as all 64 user-defined pins of the VME P2 connector. The 4292 includes a PMC module site with four standard PMC connectors, one of which also connects to the 64 pins of P2. These connections to VME P2 support various backplane I/O standards, including an extremely important one: RACEway.

Figure 3 shows the 4290 as viewed from the back plane connectors, with the four VIM processor connectors and the global bus/P2 connector identified. Note that the front panel is segmented, allowing two blank front panel sections to be removed as shown to make provisions for the front panels of VIM mezzanine

modules.

Because the VIM connectors provide such a flexible I/O solution, several different form factors have been defined for the VIM mezzanine modules. The first is the VIM-2 format shown in figure 4. It connects to two of the four VIM sites on the baseboard, providing direct I/O to two of the four processors.

Note that the front panel of the VIM-2 module is exactly the same width as a 6U VMEbus front panel. In fact, when installed on the baseboard is becomes an integral part of the front panel of the baseboard, nesting in the same slot.

Figure 5 shows two VIM-2 modules being attached to the processor baseboard.

Figure 6 shows the final assembly with two VIM-2 modules attached to the baseboard. Note that the complete assembly occupies only one VMEbus slot!

One of the major benefits of the modularity of the VIM-2 format is that the processor can be equipped with two different types of VIM modules, perhaps an input module and an output module.

Figure 7 shows an outline drawing of two VIM-2 mod-

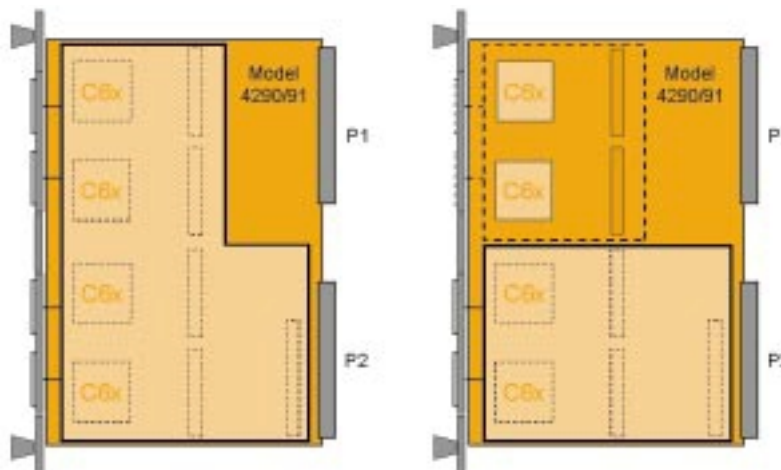


Figure 9 (left side). VIM-4R Module.
Figure 10 (right side). VIM-2R Module.

MEZZANINES

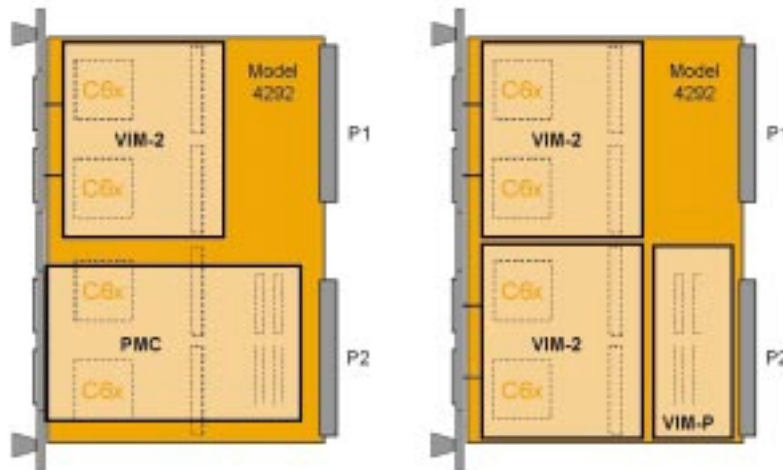


Figure 11 (left side). Model 4292 with PMC Module.
Figure 12 (right side). Model 4292 with VIM-P Module.

ules installed on a baseboard. Other VIM mezzanine form factors include the VIM-4 which provides connectivity from all front panel connectors to all four DSP's as shown in figure 8.

For the Models 4290 and 4291 only, two more VIM module formats were created to take advantage of the fifth global bus and P2 connector. The VIM-4R format in figure 9 supports a RACEway or VSB interface to all four processor nodes.

The VIM-2R in figure 10 combines the benefits of a RACEway interface for two of the processors with the ability to install a VIM-2 module for other I/O functions. This configuration can take advantage of the inter-processor pipeline FIFO's found on high-performance 'C6x boards to connect high speed front panel interfaces through a powerful DSP engine, and then out to RACEway devices for additional processing or storage.

The Model 4292 supports not only the VIM-2 and VIM-4 modules as shown in figures 7 and 8, but also allows the installation of a PMC module in place of the lower VIM-2 as shown in figure 11. The added flexibility of installing various combinations of different types of both PMC and VIM-2 modules makes the 4292 an extremely attractive platform for a large number of different applications.

For RACEway interface applications using the Model 4292, one solution is to install a RACEway adapter PMC module like the Pentek Model 7106. However, since the PMC module covers the two lower VIM connectors, only one more VIM-2 module can be installed on the processor board as shown in figure 11.

A better alternative is to use a RACEway adapter implemented in the VIM-P form factor shown in figure 12. The small module easily holds the RACEway interface circuitry contained within a single PXB or PXB++ chip. The major advantage with this approach is that now all four VIM connectors remain available to handle two VIM-2 modules or one VIM-4 module.

VIM: MODULARITY AND BANDWIDTH

Several VIM modules are currently available ranging in

function from wide-band A/D converters, digital receivers and upconverters, multi-channel A/D converters, high speed digital and FPDP interfaces and RACEway adapters. Compatible with all three 'C6x VIM processor boards, these VIM-2 modules can be installed as needed to provide application-specific subsystems with tremendous compute power and very high-bandwidth I/O.

A typical system for radar is shown in figure 13. Here a Quad 'C6203 DSP Processor, capable of 9600 MIPS peak, is equipped with two VIM-2 modules: a Model 6211 Dual Channel 65 MHz 12-bit A/D Converter VIM-2 module and a Model 6226 Dual FPDP Interface. Both I and Q analog channels from the radar system are digitized at 65 MHz. Both digitized channels flow directly through the VIM mezzanine Bi-FIFOs at 130 MB/sec into DSP A and B. After some initial processing, the data streams are passed across to DSP C and D using the interprocessor Bi-FIFOs. Finally, the processed output streams flow through the dual FPDP interface over front panel ribbon cables at up to 160 MB/sec each.

This combination of multiple, simultaneous data high-

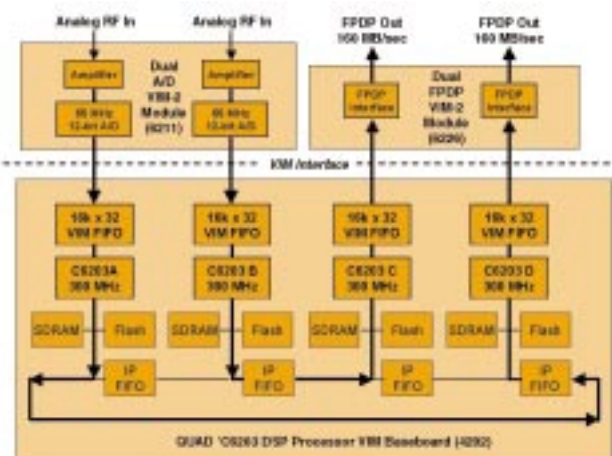


Figure 7.

bandwidth data paths with the flexibility of the mezzanine modules delivers an exceptional level of performance, all within a single VMEbus slot.

VIM SPECIFICATION

Pentek offers VIM to the market as an open, non-proprietary standard with no royalty or licensing requirements. The specification has been evolving now for nearly two years and has been used successfully by several companies to create custom, high-performance interfaces which match their system requirements to the powerful processing engine of the quad 'C6x DSP boards. The simple, direct and fast VIM connection to each of the four processors, has proven itself to be easy to use and very effective.

Already underway at Pentek, is the design of our next generation processor board, based on a radically different type of DSP chip. This design fully embraces and exploits the VIM specification to handle the even greater I/O demands of this new technology. Thus, VIM has proven itself as a truly processor-independent interface, ready for I/O tasks and processor architectures yet to be defined.

For further information, Pentek is pleased to make the VIM specification available for viewing or downloading at our website at www.pentek.com/vimspec. Pentek also welcomes inquiries from other vendors for implementation details and standardization efforts ■

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While there, he was responsible for the development of digital frequency synthesizers, FFT spectrum analyzers, and digital filter products. He designed the first commercial direct digital frequency synthesizer in 1971, and holds patents in frequency synthesis and FFT spectrum analysis techniques. Rodger has a BS degree in Physics from Allegheny College and a BS in EE and MS in EE degrees from Columbia University.