

Emulation Solutions to Reduce the Debug Cycle

Estimates for the time taken to debug a microprocessor system vary from 15 to 35 per cent of the project lifecycle. Here Richard Danter, a field applications engineer at Wind River looks at a series of products that his company has developed in a bid to reduce this time.

Debuggers have become a standard piece of kit in the software developers tool set. They are responsible for increasing the productivity of design teams more than any other development in the market during the last decade. If we take a quick look at the development of debug and emulation technology over the last 30 years it is not difficult to understand why.

Debug used to involve adding extra lines of code to a program that would output status information to a serial port and onto to a terminal. This approach was incredibly primitive since the processor would only provide the debug information that it was requested to print out.

While outputting to a terminal was okay to follow the sequence of a program when it was operating correctly, it was not particularly helpful in the primary task of acting as an aide to debugging code that contained fatal errors.

RISE AND FALL OF IN-CIRCUIT EMULATION

Parallel to the rise of 16-bit microprocessors was the development of true hardware emulators that would physically take the place of the microprocessor in the target design and truly emulate its functions providing feedback on key characteristics of the processor at the same time. This approach was called in circuit emulation (ICE) and allowed developers to monitor the status of the address and data bus and registers whilst the processor was running.

The key issue with ICE is that the emulator must run faster than the target processor in order to be able to mimic the operation of the processor and provide the additional information required. But ever increasing processor speeds and the shift to 32-bit processors in the embedded microprocessor space means that in circuit devices can no longer keep pace.

The current approach has seen microprocessor manufacturers add a specific module to their microprocessors specifically for debug purposes. Here a discrete port on the microprocessor is used to provide information about the address and data bus and the status of internal registers.

DEBUG TECHNIQUES

The choice over debug or emulator strategy now needs to be made at the outset of the design process since it has a direct impact on the target processor

selected for a design. There are currently two primary debug techniques, namely Background Debug Mode (BDM) and Joint Test Action Group (JTAG).

BDM was created specifically to provide embedded designers access to the core of the processor. It provides all the debug information required to enable the processors operation to be monitored in an embedded application. It is a technology developed essentially out of necessity allowing Motorola to target its processors directly at the embedded market.

JTAG came about by a different route. It was initially developed under the auspices of the IEEE as a standard to specify how to control and monitor the pins of compliant devices on a printed circuit board. Each microprocessor that has an implementation of JTAG has four control lines. There is a common reset and clock and two data lines which can be daisy chained to monitor multi-processor systems.

Both the BDM and JTAG protocols contain commands to read and set the values of the pins, the internal registers of devices, the address bus and the data bus. BDM can address registers on an individual basis while JTAG is slower because it reads and writes to each of the registers at the same time.

EMULATION TOOLS

Wind River has two primary emulation tools: visionPROBE shown in Photo 1 and visionICE should in Photo 2. Both applications are in their second gen-



Figure 1.

DEBUGGING

eration and support ARM, MIPS, Hitachi and Motorola microprocessors. Additional modules known as 'personality modules' allow the emulator box to support the target microprocessor.

The benefit of these approaches is that they record code execution and enable performance to be measured without interfering with the system. The intrusiveness is limited to minimal electrical load on the circuitry, program execution speed is not reduced and additional debug code does not need to be inserted by the programmer.

visionPROBE is a device that plugs into the parallel port of a PC and acts as the processing engine. The tool contains all the circuitry to convert the signals from BDM or the JTAG port of the target processor into a format that can be interpreted by the PC. The PC grabs the data and presents it to the design engineer in a graphic format.

visionICE is based around its own dedicated microcontroller which means that it can work as a stand-alone device. An Ethernet interface provides network connectivity allowing it to be accessed from a network by multiple engineers in the same design team.

In fact Wind River has a number of customers who use VisionICE remotely over a wide area network. In one instance the target processor and debug system are located in the US and are accessed over a virtual private network by engineers in Europe.

Extracting information from a target system and changing variables using a tool such as visionPROBE or visionICE is invaluable. In addition to the core features, the modular design enables the same system to be used for multiple target microprocessors protecting investment and a flash programming feature enables code to be changed almost on the fly.

CAPTURE AND ANALYSIS

But the real value of such systems lie in the ability for engineers to run live traces and model events over time. Data from the debug systems can be captured in real time and for subsequent analysis.

visionTRACE from Wind River is a module that can be added to visionPROBE and visionICE in order to provide a real time trace capability. It is currently only available for the Motorola ColdFire architecture as the trace feature is unique to BDM and is not implemented as part of JTAG.

Wind River has developed visionEVENT for JTAG specific processors. This snoops on the entire address bus, data bus and control signals while the processor is running and takes a snapshot of the system every clock cycle.

FUTURE DEVELOPMENTS

Wind River is developing its emulation tools with three specific aims: tighter integration with its real time operating systems and other development tools; improved performance throughput; and support for additional microprocessors, multi-processor systems and sys-



Figure 2.

tem-on-a-chip devices.

Tighter integration between the emulation tool and the RTOS will enable the emulator to recommend preemptive action whilst improved performance will provide greater download speeds and efficiencies in the debug process.

Ultimately Wind River will broaden its emulator support not only to include additional microprocessors, but also complete systems. As an example, Wind River is currently working with Triscend to provide emulator support for its configurable system-on-a-chip devices which combines an ARM7TDMI processor with programmable logic on a single chip.

The daisy chain feature of JTAG means that multi-processor or multi-device systems can be scanned in a single chain and individual devices in the chain can be scanned or bypassed thus making it suitable to work in conjunction with a multi-processor or system-on-a-chip device ■

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Richard has 5 years experience in embedded development, working for companies such as Sony UK, EST, and now Wind River. Previous Projects include Digital TV Set-top box design (at Sony), Optical Fibre network development and SCSI BIOS development. Richard holds an MSc in Electronic Product Engineering, and a BEng (Hons) Electronics Engineering; and in his spare time teaches Kung-Fu.