

## Solano™ Communications IC: A High- Throughput Solution for 3G Wireless and Broadband Base Stations

*This article contains perspectives on optimizing Digital Signal Processing through software-driven wide-band wireless architecture overview. As demand for third- generation (3G) wireless systems increases rapidly throughout the coming decade, the need for higher bandwidth will require ever- increasing signal processing and base station flexibility. These advances, in turn, will depend on flexible software radio architectures and on enhancements at the processing chip level.*

### OVERVIEW

**A**s demand for third- generation (3G) wireless systems increases rapidly throughout the coming decade, the need for higher bandwidth will require ever- increasing signal processing and base station flexibility. These advances, in turn, will depend on flexible software radio architectures and on enhancements at the processing chip level.

Mobile phone users around the globe want wireless access not only to more voice communications, but also to broadband "wireless web" Internet services, videoconferencing, high data- rate multimedia services, and corporate intranets. These 3G requirements exceed the limits of traditional wireless base station processing architectures. In addition, flexible software radio architectures are required for dealing with the multiple air- interface standards proliferating throughout the industry, including Wideband Code Division Multiple Access (W- CDMA), cdma2000 and the existing 2G standards.

### THE SOLANO™ COMMUNICATIONS IC

This new wireless environment calls for base station transceivers equipped with a mix of signal processing devices, including Application Specific Integrated Circuits (ASICs), programmable Digital Signal Processors (DSPs), and Field Programmable Gate Arrays (FPGAs). To alleviate the challenge of integrating this multitude of processors in a base station architecture, Spectrum Signal Processing Inc. offers the Solano™ IC. The Solano IC is an off- the- shelf solution that provides flexible, efficient communications within multiprocessor platforms.

### THE CHALLENGE: CONNECTING MULTIPLE PROCESSORS AT THE BASE STATION

Achieving efficient and flexible multiprocessor architectures for ever- evolving wireless services creates an unprecedented challenge for base station engineers. Wireless transceivers and baseband processing engines for 3G cellular base stations require a combi-

nation of IC, or ASIC, devices for high speed, fixed function processing, FPGAs for cycle- intensive programmable processing, and fixed- point DSPs for lower data rate, decision- intensive algorithms. Examples of the above include the Xilinx Virtex family of FPGAs and the Texas Instruments' C6000 family of DSPs. Base station manufacturers must interconnect these signal processing devices with the receiver and transmitter input/ output (I/ O) modules without creating bottlenecks that would seriously compromise performance.

The operation of these individual signal processors and the speed at which they can process data within a multiprocessor system continue to improve at a rapid pace. Individual processor technology, however, is not the bottleneck that prohibits or retards constructing the more complex architectures required for 3G. The bottleneck in traditional architectures occurs when moving data into, within, and out of the system - in other words, in limits on data throughput.

### WHAT'S NEEDED: A THROUGHPUT OR COMMUNICATIONS SOLUTION

What's needed is a solution that can handle the I/ O volumes of today's systems and can adapt to the demands of wireless services as they continue to evolve. This challenge is multi- dimensional. With the processing performance of individual processors increasing, elaborate base station configurations demand flexible data- flow designs and increased inter- processor bandwidth. These demands drive the evolution of new solutions that can be configured to any system requirement without compromising performance or scalability. Adding to the challenge is that a multiprocessor design must also provide for control signals and low data- rate communications paths between processors. These features enable overall system coordination and system management. This is critical in a real- time deterministic environment, such as a 3G cellular base station. Without such system management capabilities, the potential for data to be dropped is high. More and more multiprocessor architectures consist of multiple boards and potentially multiple chassis in order to achieve required processing

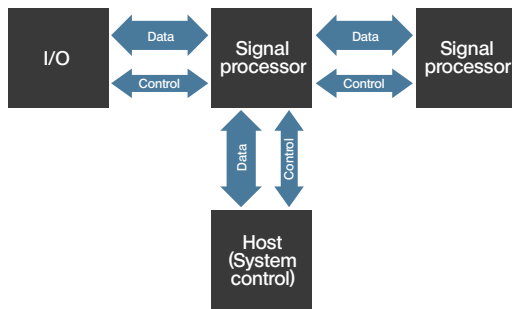


Figure 1. Communications model for interfacing processors, I/O and host in an ideal multiprocessing system, one needs to be able to provide data and control paths between a variety of signal processors, I/O and a host or system controller.

capabilities. Because of this, scalable inter-board and inter-chassis communications are also vital.

Furthermore, as systems get larger, it is often desirable for optimal DSP utilization to keep the ratio of data bandwidth to processing capability constant. In order to optimally leverage signal processing capabilities, communications solutions must consume minimal amounts of board space and only a reasonable amount of power. The architecture also must provide efficient signal processor interfaces without requiring extensive "glue logic" or extra components. Finally, 3G communications solutions must provide high-level hooks for implementing a virtualized communications scheme, along with a simple model that can give designers direct native access to the hardware.

Ultimately, any new communications solution for embedded processor systems should 1) mesh efficiently with existing system components that use other communication systems, 2) interface efficiently with next-generation processors, and 3) have the physical and electrical flexibility and expandability to adapt to new application requirements.

## ALTERNATIVE SOLUTIONS

Historically, some attempts have been made to create communications structures for high-capacity DSPs using bi-directional First-In-First-Out modules (FIFOs) or FPGAs. These implementations generally prove to be inadequate on the basis of raw bandwidth, power, design complexity and/or their lack of flexibility when confronted with the full range of systems-level communications components. In reviewing the options, it becomes clear that only a full ASIC design could provide the performance and versatility needed to increase both processor densities and broadband performance while providing an extendable base for flexible base station architecture. ASIC technology can meet a variety of requirements. ASICs can match the timing and bus loading of the external memory interface used by C6000 DSPs, Reduced Instruction Set Computer (RISC) processors, coprocessors, and FPGAs. For the physical communication channel, advanced ASIC technology offers Low Voltage Differential Signaling (LVDS) circuitry that is ideally suited to provide low power, high speed, and high noise immunity data links. These advanced technologies, tuned to the specific application, are not available with standard logic or with foreseeable FPGA devices. The ideal is a high-density, single-chip communications solution that can connect directly between FPGAs and any combination of processors at fast data rates.

## AVAILABILITY OF THE SOLANO COMMUNICATIONS IC

To meet these wireless broadband requirements and opportunities, Spectrum Signal Processing Inc., an established leader in high-performance, multiprocessing systems, has announced the availability of an ASIC-based communications solution. It is designed specifically to alleviate the challenge of interfacing multiple processors in applications such as a sophisticated cellular base station. This solution for 3G wireless and broadband multiprocessing is the Solano Communications IC.

Designed to interface with high performance DSPs,

High bandwidth data can be streamed from devices such as A/D converters to DSP's via Solano quicComm links

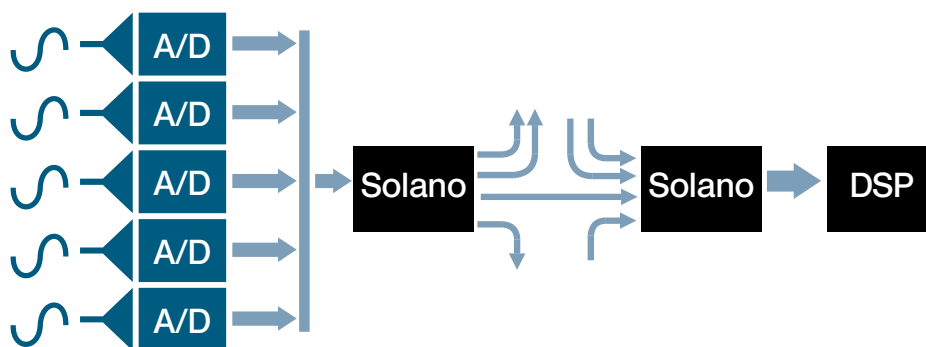


Figure 2. Example of quicComm links between I/O and DSP High bandwidth data can be streamed from devices such as A/D converters to DSPs via Solano quicComm links

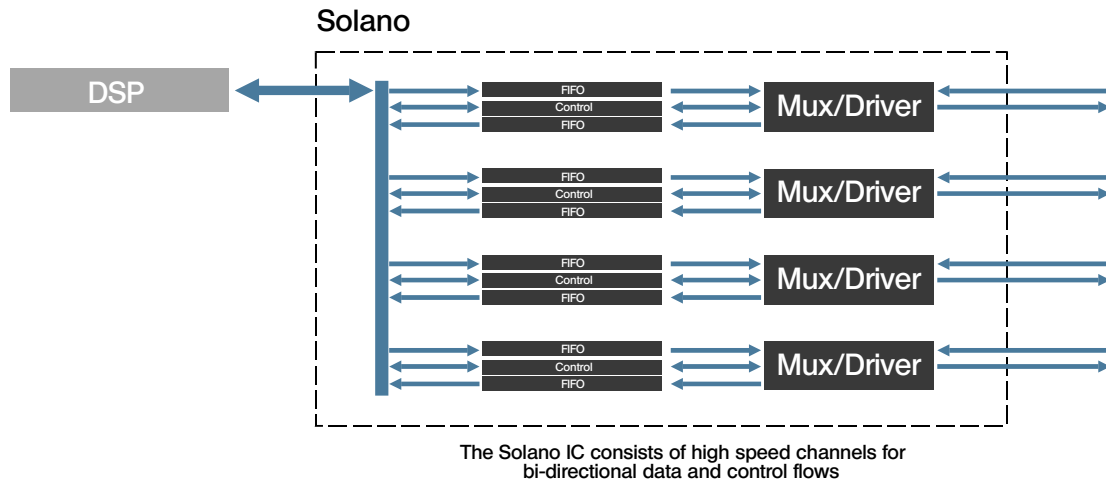


Figure 3. Block Diagram of the Solano IC architecture The Solano IC consists of high speed channels for bi-directional data and control flows.

RISC processors, coprocessors and FPGAs, the Solano ASIC contains four serial links (referred to as quicComm links), each capable of concurrently transmitting and receiving at 1.6 Gbits/ sec, for a total capacity of 12.8 Gbits/ sec. These links can be used to:

- Stream wireless data from the receivers to FPGAs for functions such as wideband CDMA de-spread-ing.
- Pass the pre-processed data from FPGAs to DSPs for baseband functions like de-interleaving and echo cancellation.
- Facilitate the flow of data through the network of processors.
- Pass data between processor boards or chassis via LVDS cables.
- Move data between the signal processing devices and the base station controller.
- Enable the output data to be streamed to transmitters.

The Solano IC is an off-the-shelf solution that offers base station engineers desirable capacity, speed and efficiencies - including cost advantages. The internal structure of the Solano IC consists of eight high-speed FIFOs, and associated control logic, that are paired up to form four full duplex 1.6 Gbit/ sec data channels. From a system designer's standpoint, each channel is as simple as a FIFO placed between the source and the destination. The Solano IC's full-duplex structure, with connections in both directions, provides robust paths for simultaneous data flow and control.

The control logic included with the full-duplex structure provides built-in circuitry for synchronization, status, control and Direct Memory Access (DMA), thereby giving Solano maximum flexibility when used for I/O-to-I/O, I/O-to-Processor, Processor-to-Host, or Processor-to-Processor communication links. When paired with a C6000, FPGA, or ASIC, the Solano IC turns that device into a multi-channel processing unit that can be directly connected to up to four other processing units or I/O devices. The Solano IC uses

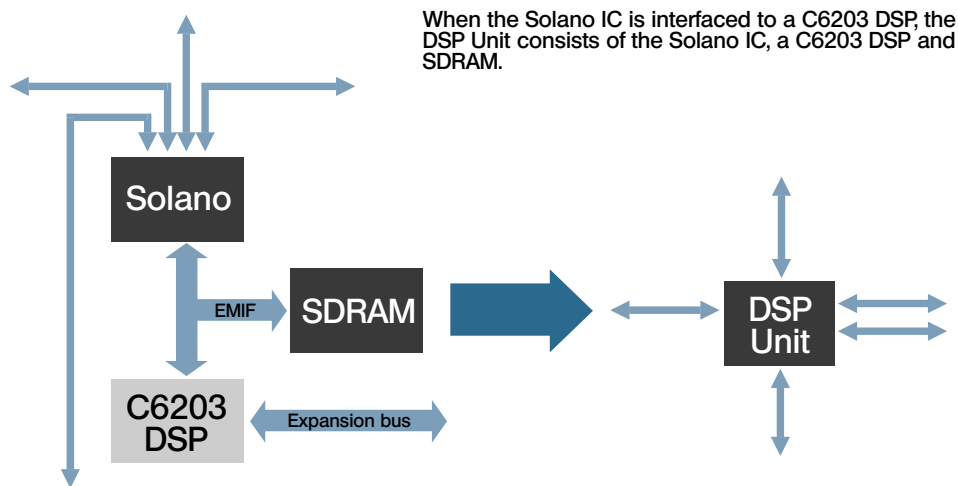


Figure 4. Example of a Texas Instruments' C6203-based DSP Unit When the Solano IC is interfaced to a C6203 DSP, the DSP Unit consists of the Solano IC, a C6203 DSP and SDRAM.

Phase Locked Loops (PLL) and design techniques available only with ASIC technologies to connect directly to the processor's memory interface at full bus speeds, while additional circuitry that monitors the memory interface usage helps to insure maximum memory bandwidth utilization. These features ideally match the Solano IC with the processor and memory to form an integral unit.

The Solano IC features a number of other benefits for base station engineering. On the communication-channel side, the impedance-matched differential structure of LVDS makes Solano relatively immune to noise, and capable of extending to longer distances. Power management is enhanced by the Solano IC's built-in ability to sense traffic usage and shut down any circuitry that is not required. By activating each of the eight uni-directional channels only during times of required usage, the number of circuits running at high frequency (including DMA, FIFOs and transceivers) can be minimized. This can keep power usage and heat dissipation to a minimum.

Notably, the combination of a Solano IC, a high-per-

formance processor and associated SDRAM together form a complete unit that constitutes a robust, flexible building block for creating any multiprocessor design.

### **SUMMARY**

The Solano Communications IC leverages the simplicity of a multiple-FIFO model into a powerful and compact device that provides system wide communications. This IC opens the door to a completely new generation of high-performance, highly-configurable and re-programmable, embedded processing for broadband services via 3G wireless base stations ■

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# **AD MICROGOLD**