

Trends in Integration - the Impact on System Designers

OMI has been at the forefront of "systems on silicon", where for high volume, consumer-type systems, cost minimisation has required very high levels of integration. The ultimate limit is a single chip, but there are a number of reasons why this may no longer be the most cost effective solution.

There are a number of trends in semiconductor manufacturing that will have a significant impact:

- increasing wafer sizes result in increasing mask costs, where the latter increase roughly exponentially. This has the effect of increasing the fixed costs (entry barrier). The number of different designs being made will probably reduce, making product differentiation harder through unique chips, or the permutations of standard chips.
- shrinking design geometries have a great impact:
 - increased propagation delays on chip result, and these will dramatically reduce on-chip bus lengths e.g. 1ns/cm will rise to 6ns/cm in 2 generations. At a typical (in 2 generations) clock frequency of 200 MHz, this is a 180 degree phase shift in 4mm, less than half the linear dimension of a relatively small chip. Possible solutions to this are a move to asynchronous operation, pipelining of buses and other techniques.
 - voltages will go down, cutting the interfacing ability. 5v I/O is possible at 0.35µm but becomes more difficult as design geometries shrink further.

Taking an overall view of chip count reduction and higher integration, a number of observations can be made:

- cost savings are greatest in the reduction from 10 chips to 2, less so from 2 to 1
- in many real systems, an interface chip will be needed to get voltage translation
- two low cost packages may be cheaper than one, more expensive, package for power considerations and/or pin count
- semiconductor yields give a "sweet spot" around 50-64mm²
 - smaller die give better yields for a given number of defects
 - at 0.25µm, the sweet spot is 1.8M gates; at 0.18µm, the sweet spot is 5.5M gates.

Can we draw any conclusions from this?

One possible outcome may be that processors will adopt a high speed serial interconnect as the standard means of interfacing to complex systems components, on-chip, as well as off-chip. Why on-chip?

Some form of decoupling (or asynchronicity) is needed, and some of the high speed protocols have been developed to have minimum overheads. The use of a low overhead, high speed, serial standard will allow multi-chip systems to be further integrated more easily when the economics allow.

OMI has been active in this area, anticipating some of these trends. The protocols have been standardised as IEEE 1355 and there are a wide variety of implementations around, including FPGA implementations. Asynchronous protocols have the advantage of working at the speed of the slowest end. This has a great advantage when mixing designs from several sources. It reduces the number of critical timing parameters, and protocols can be formally verified. Together, these can lead to a much higher probability of designs working correctly first time.

One OMI project, DIPSAP, has used this to build a chip (SMCS) to interface multiple DSPs in a signal processing system; software microkernels are available for a range of processors to support heterogeneous systems.

The bus may not be dead yet, but the time is coming closer when it becomes cost effective to use alternatives, as witnessed by the start of peripheral serial buses such as Universal Serial Bus (USB) and IEEE 1394 in the PC world. Predictions are always dangerous in this business, but there are a number of compelling technical reasons why high speed serial interconnect will have a substantial impact on systems design in the remainder of this millennium, and OMI, and the companies involved, will have led the way.

Anyone who wants to know more should contact the "1355 Association", which can be found at <http://www.1355-association.org>



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