

# Designing a Dual Pentium II SBC

*I-Bus, Inc. builds passive backplanes, CPU boards, and enclosures for the industrial PC marketplace. Passive backplane technology relies on a Single board Computer (SBC) to provide the processor function that is normally on a system board (i.e., a motherboard). An SBC is the size of a full length PC-AT card. The interface for ISA and PCI is defined by the PCI Industrial Computers Manufacturer's Group (PICMG). PICMG controls the connector edge specification for SBCs. This technology is used to provide a high degree of serviceability and ease of upgrade for the customer. For example, one need only replace the CPU board to upgrade a processor, as opposed to removing all installed add-in boards and replacing the system board entirely.*

**W**ith the introduction of Intel's Pentium II processor, the design of SBCs has changed dramatically. From 8088 to Pentium Pro, a socket was always used and contained the entire CPU in one small package, such as a Pin Grid Array (PGA), for 286 and above. However with the Pentium II, the Intel design has evolved into a Single Edge Contact (SEC) cartridge. The SEC contains the processor and cache on a circuit board, which is inserted into an edge connector placed on the system board. This allows Intel a greater flexibility in their choice of cache, and it is expected to reduce the cost of the processor module over time. However, it also places certain restrictions on SBC designers due to the size of the SEC (indeed, the overall dimensions of a Pentium II are approximately 5.6"x1.9"x2.5"). Such a large size has caused a complete re-design of the standard layout of I-Bus CPU boards using the Pentium II, the first of which is called Nautilus.

Current I-Bus CPU boards place the Single Inline Memory Modules (SIMMs) and processor chip towards

the front of the enclosure to capture the cool inlet air generated by system fans. This placement is important because cooler processor chips means increased reliability. However, in light of the large size of the Pentium II, our Mechanical and Electrical engineers consulted with each other to determine what physical restrictions were required and what was the best course of action. When all was said and done, the basic design criteria we used to lay out previous SBCs had to be abandoned with the Nautilus. But amidst the criteria discarded, one requisite remained: the board must be available as an upgrade for current products. This requirement drove much of the design work, which made Nautilus what it is today.

## THE EVOLUTION

The Nautilus SBC design was based on the I-Bus Thresher Pentium Pro CPU board, a well-tested and proven design. First, the mechanical layout of the Pentium II module was recreated in the Computer Aided Design (CAD) system, using mechanical data provided by Intel. SBC components typically cannot be placed according to the Intel design guidelines. This is due to the narrow width and long length of an SBC (4.5"X 13.4"). However, in this case the SEC package allowed the design to much more closely follow Intel's layout guidelines, which would reduce routing conflicts.

Next, the Thresher schematic was altered to include two processors. Each Pentium II processor has on-board resistor terminations, which are required for proper operation of the Gunning Transceiver Logic (GTL) bus. However, a two-processor approach eliminates the need for on-board resistor terminations. This simple fact alone greatly improves the routability of the board, since the GTL bus termination power has only to be delivered to the processors instead of feeding a total of 64 resistor packs placed on the solder side of the PCB. At this stage of design, a second Voltage Regulator Module (VRM) socket also was added to provide power to the second CPU.

## THE LAYOUT

With the initial design complete, preliminary layout was begun. It was quickly evident that the 2 VRM idea was not going to be possible because the PCB real estate required for this power solution was not available. Thus, we were forced to design on-board VRMs, result-

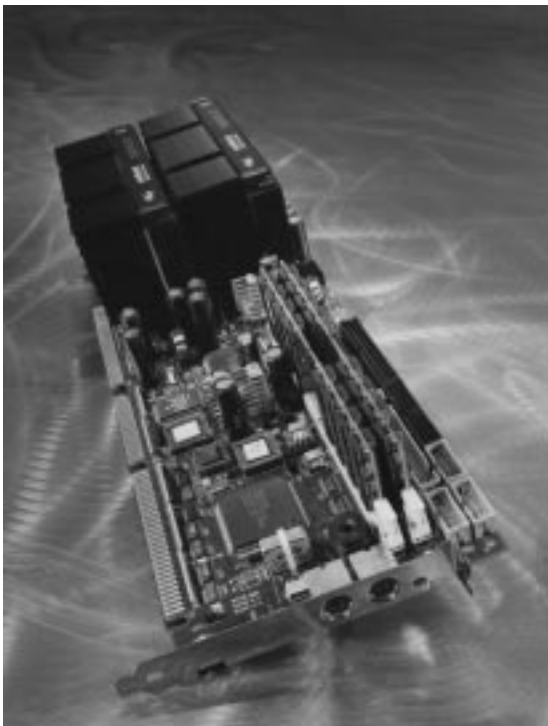


Figure 1. Nautilus SBC

ing in time lost searching for a cost effective and easy solution for powering the two processors. Eventually, and due to a concern about the overall power consumption of the CPU, a synchronous controller was chosen from Linfinity to attain the maximum efficiency from the CPU power supplies.

After the on-board power supplies were designed in, there remained a problem with PCB real estate. To keep Thresher's four SIMM design would preclude adding standard PC I/O (serial and parallel ports, and disk drive interfaces) to the board. We therefore made the decision to convert the four, 5 volt SIMM sockets into two, 3.3 volt unbuffered Dual Inline Memory Module (DIMM) sockets. This created a large increase in available board space.

However, the added complexity of 3.3-volt DIMMs caused a problem in the power supply area. The previous design used a linear regulator to provide 3.3 volts for the Intel chipset and to support circuitry. Adding two DIMMs would necessitate a more efficient power supply alternative to reduce heat dissipation and overall power consumption. We therefore chose a switching power supply solution by using the Unitrode UCC3813, which provides >10A output current while remaining cost effective in terms of overall CPU board expense.

With all these changes in place, the design could now be contained on an SBC with room to spare. As a result, a Symbios Ultra2 Wide SCSI processor was added to the board to offset the loss of add-in board slots due to the size of the Pentium IIs and DIMMs.

With the layout now complete, the daunting task of routing an SBC with three switching power supplies and two Pentium IIs with GTL technology lay ahead. It is important to note here that in order to simplify the overall task of SBC design, layout, and routing, I-Bus engineering uses Mentor Graphics CAE tools because they provide a great deal of flexibility and control over the board design process. For instance, the design entry tool allows the engineer to incorporate routing specifications into the schematic at the time of design. Because this tool permits the inclusion of so much information, there is less risk of forgotten or misinterpreted data between the CPU designer and the PCB designer.

### MENTOR NET TYPE RULES

Another example of a routing specification that can be included on the schematic are Mentor Net Type rules. These rules control the available routing layers, width of the trace, spacing between adjacent traces, and layers of the PCB available for routing. This feature can prevent GTL+ signals -- which have a 1-volt peak-to-peak swing -- from being routed next to other signals, causing undesired coupling. A wide trace net type property is defined on power nets such as +5V, +3V, and Ground to insure that all surface mount components have an adequate connection to the PCB power plane. Controlling the length of critical traces, as is necessary to equalizing the lengths of the 66MHz clocks for the chipset and processors, is accomplished by adding a property to these nets on the

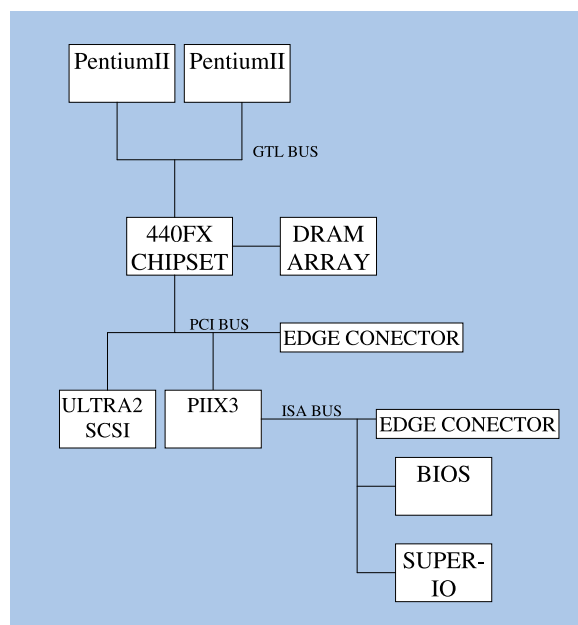


Figure 2. Nautilus Block Diagram

schematic, which specifies the minimum and maximum allowable length.

### ELECTRONICAL GLASS RULES

More complicated signal routing is controlled by Electrical Class rules defined in the schematic and attached to the appropriate nets on the design. These rules allow the user to define a topology, which controls the order in which the nets are connected by the autorouter. The Net Type rules are used in conjunction with Electrical Class rules to control the available routing layers, width, and spacing of traces. The main groups of signals using Electrical Class rules are the GTL+ bus signals, which go from the CPUs to the chipset. In order for the CPU bus to operate correctly, the signals must travel in order from one processor to the chipset and then to the other processor. Furthermore, there are minimum and maximum distances allowed between nodes on the net that can be defined with the Electrical Class rule.

Mentor Graphics can also control the stub length from any node to the main trace. This flexibility removes the burden from the PCB designer to manually route the approximately 128 signals associated with the GTL+ bus.

### DIFFERENTIAL PAIR PROPERTY

Another important feature of Mentor software is the Differential Pair property. This property was used in the layout and routing of the Ultra2 SCSI bus. When this property is attached to pairs of signals, it forces the autorouter to route them next to each other from the source to the destination. This was very useful in routing the SCSI data and control signals from the SCSI processor to the terminator and then to the connector, and it saved our PCB designer from manually routing 25 pairs of signals.

## ROUTING

With the layout complete and the electrical class and net type properties in place, the Cooper and Chyan gridless router took over. Over the years, we have developed a script for routing SBCs. Due to the narrow width and long length of the card, routing is typically much more difficult than with a motherboard. Nets are prioritized according to criticality before the autorouter is started. The autorouter can make as many passes as necessary, but we can usually tell in approximately 25 passes whether the board layout will allow routing completion or if it requires more refinement. Nautilus took about 16 hours on the autorouter, and was one of the easier designs to route. Of course, after the autorouter is finished, there is always some cleanup work to do. But the bulk of the routing was completed automatically, and overnight.

## THE SIMULATION TOOL

With routing complete, work was started on the simulation. The goal of the simulation tool is to show us what the signals look like on the PCB even before the board is fabricated. The better the data that is used, the better the simulation results. We use numbers obtained by our PCB fabrication house for the dielectric constant of fiberglass (FR4) and the conductivity of copper. The simulator requires that we specifically enter a thickness of FR4 and a copper weight of 1/2oz., 1oz. etc. for each layer of the circuit board. The frequency of operation is also specified along with a time step used for convergence of signals.

The Nautilus board contains 10 physical layers. Once the physical layers are complete, the models provided by silicon vendors are converted by an IBIS to XTK translator to the XTK format needed by the tool. We generate the models required but not provided by IC vendors. When all models have been converted and compiled, the database is checked and missing models are reported. Once we are satisfied that all models necessary are present, the field solver is invoked to calculate the crosstalk and signal characteristics. This process is usually done overnight since crosstalk results are requested from several adjacent layers on the PCB.

The simulation tool provides an interactive simulator for viewing each signal as it traverses the path on the PCB. Not all signals are studied on the design. However, the GTL+ signals are scrutinized to insure that Intel specifications are met. Others, such as clocks and memory interface signals, are verified as well. Any problematic ones are touched up manually in the PCB layout and the simulation is re-run. The touch-up work is minimized by the use of the electrical class properties defined early on in the design process.

Once the simulation has been verified, the design is sent out for fabrication and assembly. All three processors designed by engineering and verified using the simulator worked as first prototypes with no changes to any signals on the GTL bus. This gives us great confidence in the simulator and the parameters we are using to verify the designs before fabrication.

The new CPU design from Intel created a variety of challenges, especially since very few companies utilize the design restrictions I-Bus demands. With input from our mechanical engineers, our electrical engineers produced a high quality CPU board with good airflow over key components. The Nautilus is the first in a series of I-Bus Pentium II designs.

## SBC'S FOR REAL-TIME APPLICATIONS

Thanks to performance improvements in dynamic execution, multiple branch prediction and data flow analysis architectures over the Pentium Pro, and to the addition of MMX functionality, the Pentium II becomes very valuable in applications where intense computational functions are performed, such as those involving pattern recognition using neural network calculations. For example, high-speed image processing functions used in optical character recognition applications or friend-or-foe recognition for military intelligence were formerly handled by co-processor boards. As a result, these functions can now be handled directly by a Pentium II microprocessor. Similarly, voice recognition capabilities, which make possible enhanced telecom services such as automated attendants or sophisticated personal assistants, are now benefiting from the power of Pentium II processors by offloading part of the voice recognition algorithm processing to the CPU. In other words, system price may be reduced by utilizing the CPU to perform certain application-specific functions that previously required a dedicated processor. Another notable advantage of CPU boards based on the Pentium II is the upgrade path, both in terms of processing speed (over and above to 300MHz) and multi-processing (by simply adding a second Pentium II cartridge). ■

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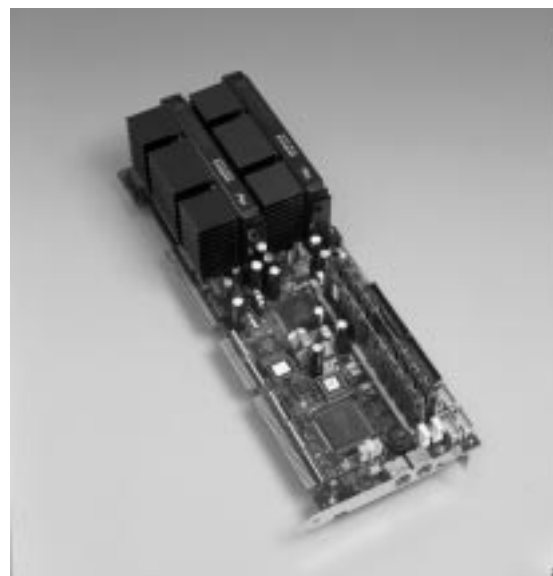


Figure 3. Nautilus SBC