

# Mezzanines Cards Enhance Versatility, Maximize Benefits of CompactPCI

*The flexibility and compatibility benefits of CompactPCI, combined with complementary mezzanine buses are expanding functionality and positioning cPCI as the leading bus platform in a wide range of embedded applications. Many of the early mezzanine boards were developed by VME manufacturers looking to maximize bandwidth and functionality. Today, the premier high-end mezzanine solution is PMC (PCI Mezzanine Card), which continues to dominate the market as the industry relies more on mezzanine platforms to eliminate the need for customized hardware and reduce the number (and cost) of individual I/O boards.*

*This article examines some of the advantages of PMC on cPCI, as well as looks at the use of secondary bus technologies that are also helping to bring major cost and time-to-market benefits, particularly in real-time applications.*

Combining the benefits of the PCI desktop architecture with the ruggedness of the Eurocard form factor, CompactPCI continues to penetrate embedded applications at a rapid rate. PC-based applications like computer telephony integration are ideally suited to take advantage of the plug and play benefits of CompactPCI, allowing designers to use the wide range of low-cost, off-the-shelf peripherals and application software that has been developed for the PC market.

While CompactPCI brings a host of flexibility and compatibility benefits, new definitions to the cPCI specification and implementation of complementary sub-buses and mezzanine buses such as PMC (PCI Mezzanine Card), are enhancing functionality and helping to establish cPCI as the leading bus architecture in a wide range of embedded applications.

Mezzanine boards are not new in the open-bus standards-based world, having been used for a variety of functions, more often to add functionality or increase functional density of a standard board. Many of the early mezzanine boards were developed by VME hardware manufacturers looking to maximize bandwidth while addressing a wide range of applications without having to design a new board for each one. While these semi-proprietary boards enjoyed some early success, they also carried some drawbacks, including limited silicon choices and the resistance among manufacturers to agree on a common mezzanine bus standard (at one time there were close to 30 different mezzanine platforms for VME).

Among the early leaders in mezzanine platforms was IndustryPack, which first began appearing on a variety of host VME boards, and ultimately became an ANSI standard. IndustryPacks offer a compact formfactor

(about half the size of PMC modules) and can be implemented in single or doublewide configurations. As such, IPs have become the platform of choice where space is limited, or where many different functions are required. For example, it's possible to select a number of different IPs to provide various types of I/O (speed, width or protocol) from a single board. While the form factor works to the advantage of the IP in many applications, in other cases it is a drawback. For example, there is no provision for front-panel I/O in the IP specification, which is critical in some applications.

In the late 80s, the PC/104 module gained rapid acceptance as a mezzanine I/O module for VME, STD and stand-alone single board computers. However, because of the PC bus' incompatibility with the 68K-processor family, very few VME manufacturers could use the PC/104. Nevertheless, the mezzanine did serve duty as an effective platform on other buses and standalone SBCs.

Certainly, the most significant chapter in the mezzanine bus story is the adoption of the PCI (Peripheral Component Interconnect) specification. PCI and its variety of configurations have penetrated deeply into embedded markets as manufactures leverage the low prices of PCI interface chips, driven by the volumes of the desktop market. Since its official introduction in 1992, PCI has been integrated in a wide variety of form factors including an on-board local bus, a board/connector bus, system-bus in passive backplane and CompactPCI configurations, as well as a mezzanine or peripheral bus.

Among the newest PCI-based standard gaining rapid acceptance from system bus to mezzanine bus is PC-MIP. The smaller PC-MIP form factor (47mm by 90mm) enables modules to fit on both Eurocard and desktop

PC boards. The mezzanine card is designed for both front- and rear-panel I/O, and offers a form factor that allows as many as six PC-MIPs on one, single-high 6U card.

Still, the premier high-end mezzanine solution is PMC, which continues to dominate the market as the industry relies more on mezzanine platforms to eliminate the need for customized hardware and reduce the number (and cost) of individual I/O boards. Today, nearly every new CPU board design includes PCI as a local bus, and most include PMC slots.

## PMC ON CPCI - A POTENT COMBINATION

The technical advantages and design flexibility of PMC, combined with the rugged formfactor and system compatibility of CompactPCI, results in a dynamic mix of capabilities. CompactPCI merges the electrical, logical and software standards of the PCI bus with the Eurocard format and high-density, industry-standard (IEC 1076) 2-mm pin and socket connector. The modular, passive backplane architecture shares the same processor and software base as industrialized PCs, resulting in the best silicon support and access to low-cost PC peripherals, interface components and an abundance of plug and play software - a significant advantage when time to market and cost issues are a factor.

PMC boards offer greater functionality due to their modularity and ability to take advantage of the wide range of chip-level components available for the PC market. Secondly, using PMC modules instead of separate cPCI boards frees up one or more slots, providing a lower cost solution than a system slot board. Finally, as interface boards, PMC cards give system designers the flexibility to provide a number of interfaces such as digital and serial I/O interfaces, analog-

to digital, digital-to-analog, as well as optically isolated interfaces.

The PMC architecture is an open IEEE standard, (P1386 and 1386.1) which has been rapidly adopted by many board-level designers, both on open buses like VME and CompactPCI, as well as on proprietary bus boards. PMC is electrically identical to PCI, the high-speed local bus being used in most new PCs today. However, while the PCI specification defines a 10.7cm x 29.52cm board to plug into a personal computer motherboard in a perpendicular fashion, PMC modules are 7.4cm x 14.9cm and are mounted parallel to the base board, such as a cPCI single board computer.

With significant rear I/O capacity and available PCI bus bandwidth, PMC offers significant design flexibility for embedded systems. Designers can build modular, scaleable systems that can be easily upgraded by replacing the old board with a newer design without changing the basic system architecture. Additionally, virtually all-new processor board designs support PCI as the local bus, and can therefore easily support designs with PMC expansion.

The open PMC standard allows equipment buyers to purchase modules with a variety of different communications interfaces, thereby changing the "personality" of a baseboard depending on what PMC modules are applied to it. For instance, application-specific functionality such as SS7 links, LAN interfaces and WAN interfaces, can be added to the "generic" base boards using PMC modules at a much lower cost than a separate cPCI board. The PMC bus can also be employed in proprietary systems, allowing the proprietary architecture to be used for communication between boards within the system, and the PMC boards to add application-specific functionality.

Sufficient bandwidth is critical to support high-speed

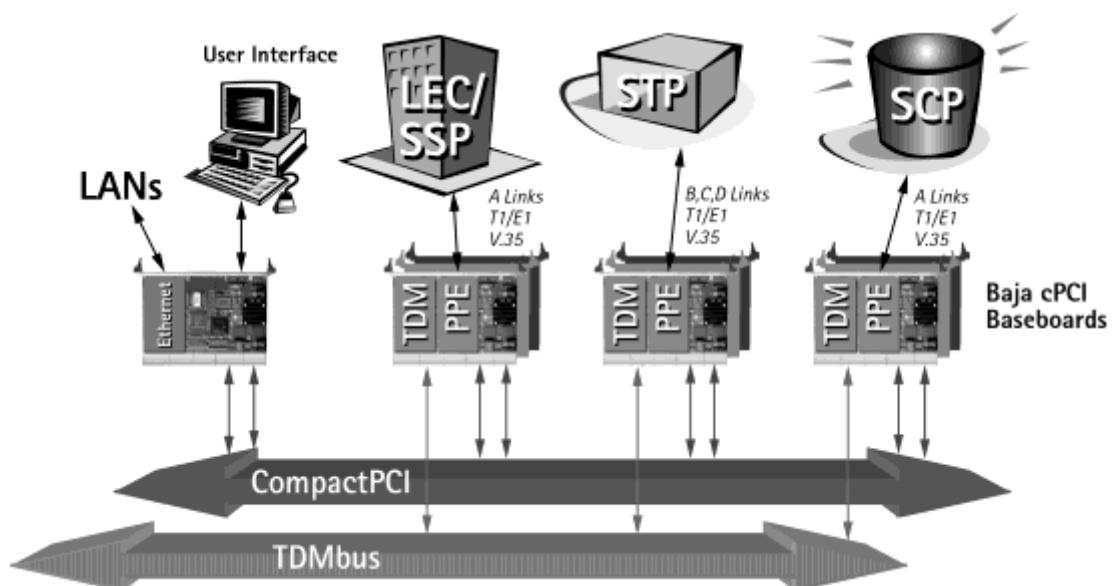


Figure 1. PMC on CompactPCI

telephony applications such as video, Internet access and voice/fax. A derivative of the PCI standard, PMC features a 33 MHz synchronous bus with either a 32 or 64 bit data path and transfer speeds approaching 264 Mbytes/sec. This gives communications system designers the high-speed bus access they increasingly require for connecting high-bandwidth peripherals and intelligent controllers.

The incorporation of PMC modules as part of a tightly integrated hardware/software subsystem solution is helping telecom OEMs dramatically shorten development cycles and reduce costs. For example, the Portable Protocol Engine (PPE) from Artesyn Communication Products, is a hardware/software subsystem that simplifies development of SS7 and HDLC links. The PPE combines dual PMC modules with a user API (application programming interface) and a choice of protocol options, enabling system designers to employ a single hardware/software platform for multiple network applications, minimizing integration problems, spares issues and application interface concerns. This solution significantly reduces time to market, insulates the customer from changes in hardware due to updates or changes and allows the customer to focus on application rather than low level porting.

PMC boards also don't use any of the bus bandwidth or consume a bus slot, an important consideration in many embedded systems. As a result, bandwidth can be reserved to synchronize processes between intelligent cPCI boards rather than as a means to move large blocks of real-time data to and from the processor board.

### SECONDARY BUS SOLUTIONS

Using standard bus-based technology like CompactPCI and PMC in the design of high-speed telecom systems can bring major cost and time-to-market benefits, but it does have some limitations, particularly in real-time applications. Since PCI is a non-deterministic network, in telecommunications (particularly voice) and multimedia applications, data arriving with unpredictable timing sounds garbled or choppy. Therefore, while CompactPCI is an ideal control bus in these applications, it is less than ideal for delivery of voice data.

A key requirement in processing telephony data such as voice or video is the implementation of a secondary bus for handling the transfer of real-time data, independent from the control data being processed across the system bus. Typically, a subsystem bus like a time division multiplexing (TDM) bus is integrated into the design to handle real-time voice or signal data. While a number of proprietary methods have been used for this type of signaling on different platforms, they required the use of proprietary cards or employed competing bus architectures.

The emergence of the H.110 Computer Telephony bus specification, (released last Spring by PICMG, working with the ECTF [Enterprise Computer Telephony Forum]) is a significant step toward establishing CompactPCI as the preeminent bus for system development in the computer telephony field. As a derivative of H.100



Figure 2. Baja CompactPCI

which defined a TDM bus in a PC environment, H.110 specifies a single backplane-based signaling specification for telephony applications, (the J4 connector is specified for routing the H.100 CT bus on the cPCI backplane; the J5 is specified for additional telephony I/O) further enhancing the open, standards-based benefits of cPCI. For example, network designers can employ the H.110 bus as a switching fabric to route calls with a base station controller, or use the bus within a STP (signal transfer point) as a switching fabric for SS7 network communications.

H.110 offers the same physical features as H.100, including 64 Kbs data rates, up to 4096 bi-directional time slots, and bit rates up to 8.192 MHz. The full 32-bit bus implementation provides 262 Mbit/sec. of total bandwidth. The primary difference is that H.110 has extensions for CompactPCI and it supports the CompactPCI Hot Swap Specification. By combining the telephony-oriented features of H.100 with the mechanical advantages of cPCI over the standard PC architecture, H.110 becomes the preferred solution for complex, easy to maintain computer telephony systems, such as voice mail and interactive automated phone attendants.

The rapidly changing face of the communications industry and the pressing demand for new services continues to challenge technology and products as designers look to differentiate themselves for increased revenue and market share. While cPCI may have been initially viewed simply as PCI architecture in a rugged formfactor, new bus standards and complementary mezzanine options like PMC, are significantly enhancing functionality, easing the system design task, shortening design cycles, and helping to further establish cPCI as a leading contender in the embedded market. ■

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