

Hyperstone E1-32X RISC/DSP

Single-core RISC/DSP processors for low cost embedded multimedia and Internet enabling systems

The article describes the hyperstone unified RISC/DSP processor architecture for embedded systems and DSP applications. High-volume customers for hyperstone RISC/DSP processors are mainly in the area of digital still cameras, fingerprint recognition systems, telecommunication, hand-held Internet enabling devices. Peak performance of the hyperstone E1-32X RISC/DSP is 80 MIPS and 240 million operations per second (MOPS). Among others, the chips include an integrated memory of 8 kBytes, a bus interface for glueless connection of memory and periphery, and a PLL. Power consumption of the hyperstone E1-32X is as low as 80 mW at 2.7 V and 50 MHz.

INTRODUCTION

Hyperstone electronics has introduced its new "X" series of unified 32-bit RISC/DSP processors for embedded systems and DSP applications. Peak performance of the hyperstone E1-32X is up to 80 MIPS and 240 million operations per second (MOPS). Among others, the chips include an integrated memory of 8 kBytes, a bus interface for glue-less connection of memory and periphery as well as a PLL. The power consumption of the hyperstone E1-32X is as low as 80 mW at 2.7 V and 50 MHz. Two power-saving modes are implemented: The power-down mode stops instruction execution, while DRAM refresh and the internal timer remain active. The other power-saving mode, sleep-mode, turns off everything, thus reducing current consumption to 30 μ A.

The unified RISC/DSP approach means that all instructions, including the DSP instructions are strictly following RISC principles. As a result, programming is very easy by using ANSI C and a dedicated DSP library, which utilizes the parallelism between ALU, DSP and Load/Store unit in the hyperstone architecture. Hyperstone E1-32X RISC/DSP processors are shipping in volume as stand-alone units. Also, a single-core RISC/DSP macro cell is available for ASIC integration. All development tools are directly supplied from hyperstone. Software from 3rd parties include a JPEG library, scaleable OS, Windows 95 / NT based debuggers, and others. High-volume customers for hyperstone RISC/DSP processors are mainly in the area of digital still cameras, fingerprint recognition systems, telecommunication, and hand-held Internet enabling devices.

Nowadays, numerous applications in the area of telecommunication, Internet Hardware and other electronics consumer products need powerful controller

chips as well as digital signal processing. This paper shows the approach of hyperstone electronics to combine a RISC processor and a DSP in a unified architecture.

TRADITION OF RISC AND DSP

In the past, RISC and DSPs have been evolved separately from each other, resulting in very different architectures. While RISC processors are register-oriented with a load/store architecture, DSPs are memory-oriented with specialized architectures. RISC processors usually also have caches for instructions and for data, whereas traditional DSPs have instruction buffers and on-chip RAM. Last, but not least, where RISC processors have general purpose units running at high clock frequencies serving general purpose tasks, DSPs have dedicated units running at moderate frequency with high sample rates, serving dedicated applications. There are other differences as well, and it should be obvious that the design of an efficient combination of these totally different kinds of products is a challenge for those engineers who meet this task.

Hyperstone's method to combine RISC and DSP

What methods can be imagined to combine functions of a RISC processor and a DSP in a system?

The easiest way is to use a standard Controller and additionally a separate DSP. However, these chips have totally different architectures, as mentioned before. As a result, it is very cumbersome to integrate these chips into a system. For example, a lot of separate logic is required to connect external memory or peripheral devices to both processors. Additionally, data exchange for controller and DSP tasks is limited

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by the bottleneck in between them. On the software side, the developer has to deal with two sets of operating systems (OS) and development systems, which can be source for many problems. Additionally, it might be necessary to pay license fees for these two OS. Moreover, power-down mechanisms have to be programmed and synchronized.

Another method to serve controller and DSP demands in a system is to integrate a RISC core and a DSP core into one piece of silicon. In that case, the total footprint is less compared to the previous example. However, similar problems with OS and development tools, data bottlenecks and integration into a system remain.

The most consequent way to integrate controller and DSP functions is the full architectural integration, as implemented in hyperstone's RISC/DSP processors. The unified hyperstone E1-32X RISC/DSP is an example of how a RISC-based DSP concept has been implemented. First processors of this type have been introduced at the end of 1995, and the third generation is in production already.

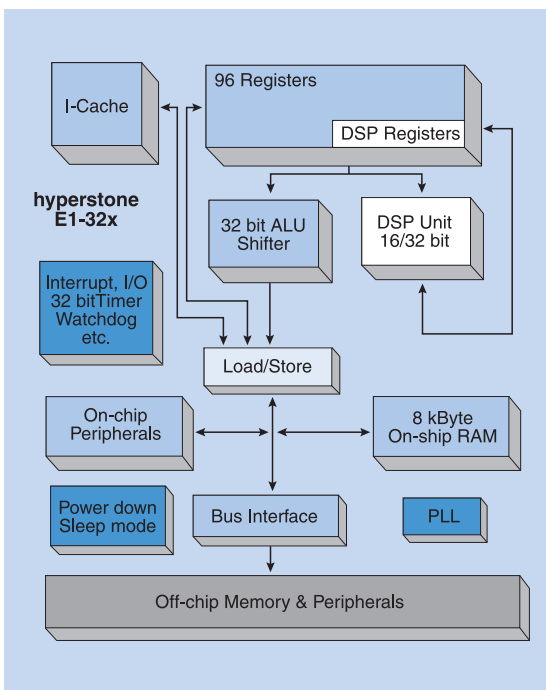


Figure 1: hyperstone RISC/DSP block diagram

The hyperstone RISC/DSP architecture provides a large set of 96 registers. It offers a set of instructions with variable length of 16 bit, 32 bit and 48 bit, resulting in high code density. The instruction length varies in a program and is automatically determined by the operands, so that the programmer does not need to care about. The processors are based on a 32-bit RISC and a 16/32-bit DSP combined in a single-core full architectural integration. All instructions are strictly working on RISC principles, including DSP instructions. All operands are transferred from internal or external memory to the register set by means of the load/store unit. ALU as well as DSP take their operands only from the register set. After execution, the results of either unit

are stored back to the register set. This concept implements that results from one unit can automatically be operands for the other unit and vice versa. This means also that an extra communication path between ALU and DSP is superfluous because communication is inherently carried out through the register set. ALU, DSP unit and load/store can work in parallel. For example, at the same time when ALU and DSP are busy, data transfer from or to memory can take place. The DSP unit is implemented as a 16 x 16 bit multiplier and a 48 bit adder. It also can process 32 bit operands into a 64 bit accumulator implemented by concatenating two 32 bit registers.

An 8 kByte RAM for data and instructions is integrated, as well as an instruction buffer. A PLL multiplies the external clock by a factor of 0.5, 1, 2, or 4. This factor can be determined dynamically by dedicated register settings, so that the system can be optimized with respect to speed and power consumption, even dynamically during run-time of a program.

Using the on-chip bus interface all memory and periphery devices can be connected directly to the processor. The address range is 4 GByte in total and is available for logical instructions as well as for DSP instructions. A power down and a sleep mode are also integrated, as well as timers and interrupt control logic.

The hyperstone architecture is extendable, which means that additional execution units can be added just like the DSP engine has been implemented. This can be useful when special hardware for accelerating certain functions is inevitable.

Parallelism between DSP unit, ALU, Load/Store unit

The parallelism between DSP unit, load/store unit and ALU is shown in the following example. In each cycle, one instruction can be issued. The DSP unit is busy with executing a multiplication with complex 16 bit operands. Since the DSP unit is based on a 16x16 bit

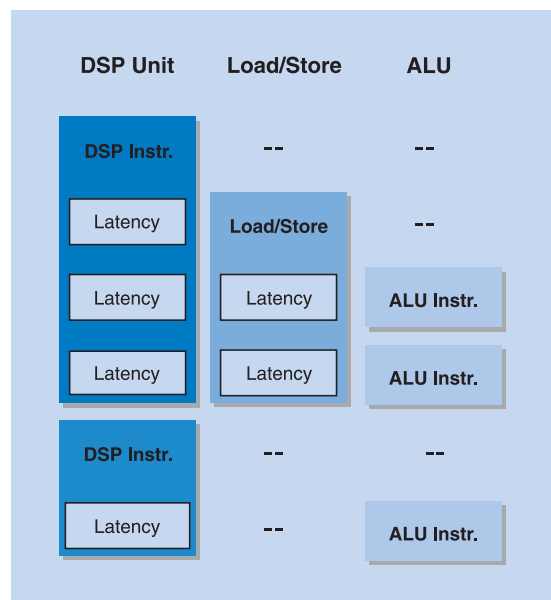


Figure 2: Parallelism between DSP, ALU, Load/Store

multiplier, this particular multiplication requires more than one cycle, the so-called latency cycles. During latency cycles, other execution units can become busy. After issuing the DSP instruction, another execution unit can be activated, for example the load/store unit for loading data from a slow and cheap external memory. In the next cycle, the ALU can be activated for logical calculations, such as shift or address calculation or loop control. At this time, all three units are active, thus 3 operations are executed within one clock cycle.

In order to utilize this parallelism of the hyperstone RISC/DSP architecture, a DSP library has been developed, containing more than 130 functions, such as FFT, digital filter calculations, Cosine transform, multidimensional arithmetic and the like. The library has been optimized in Assembly language and can be accessed from ANSI C very easily just by passing parameters and retrieving the results. Hence, the programmer does not need to take care how the parallelism is working internally.

Long list of DSP instructions

The DSP instructions of hyperstone RISC/DSP processors are far more than just Multiply-accumulate (MAC). They include multiply with 16 and 32 bit real and complex operands, 16 bit and 32 bit MAC and multiply-subtract, MAC with complex 16 bit operands, add/sub with 16 bit complex numbers for Fast Fourier Transform, and others. Depending on the operands, latency cycles between 1 and 4 cycles are required to obtain the results, which may vary in length as well. As mentioned above, other operations can be executed in parallel to the latency cycles.

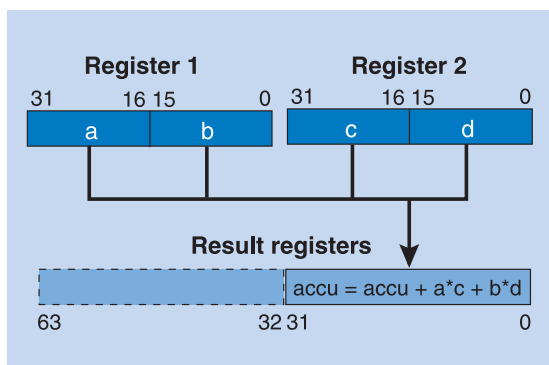


Figure 3: Subword Processing

The hyperstone RISC/DSP processors also provide subword processing. This means that one 32-bit register may contain two 16-bit operands.

As a consequence, two 16-bit operands can be captured within one cycle for execution in the DSP unit. An example is a multiplication with complex 16-bit operands where the real part is in one half of the register and the imaginary part in the other half of the register.

In case that the result is 64 bit, two 32-bit registers of the architecture's register set are concatenated.

SPECIFICATIONS AND PERFORMANCE DATA OF HYPERSTONE E1-32X RISC/DSP

- 80 MHz @ 5V, 80 MIPS, 240 MOPS
- 1 k CFFT in less than 0.5 ms
- Power-Down Current < 1.1 mA @ 2.7 V
- Sleep Mode Current < 100 μ A
- 8 KB on-chip RAM
- 80 mW @ 50 MHz (2.7 V)
- 700 MIPS / Watt
- 16 mm² total die-size excl. pads (0.5 μ m 2 ML CMOS)
- Packages: 144 pin TQFP, 100 pin TQFP, 160 pin QFP
- Also available as Verilog Macro cell
- Shipping in volume

This table shows specifications and performance data of the hyperstone E1-32X RISC/DSP processors. Right now, the die-size of the silicon is 16 mm² excluding pads in a 0.5 μ m CMOS logic process with 2 metal layers. A process with smaller geometry would pad-limit the present implementation of the hyperstone E1-32X. However, hyperstone will also switch to 0.25 μ m processes in future and implement additional functionality. Hyperstone is selling the complete chips ready for PCB mounting, as well as a Verilog Macro cell for ASIC implementation.

SYSTEM DEVELOPMENT TOOLS

For system development a complete set of tools is available from hyperstone electronics, including C Compiler, Assembler, Real-time OS, DSP library, profiler, source- and system-level debugger, system configuration tool, and others. Additional tools are available from 3rd party companies, including configurable real-time systems, integrated development environments running on Windows 95/NT, JPEG, optical character recognition, fingerprint recognition, communication protocols, web-browsers, speech codecs, MP3, soft-modems and others. This list is continuously extended.

SYSTEM DEVELOPMENT FLOW

The design flow for systems utilizing hyperstone RISC/DSP processors is as follows: The system development board consists of a hyperstone E1-32X, 4 MB DRAM, 128 kB SRAM. The board also has two I/O expansion connectors providing all hyperstone signals. The development board is connected either with the ISA bus of the PC or with a serial link.

Using the two on-board connectors, the customer can connect his own dedicated application to the hyperstone development board. This may be a hardware that is implemented on a breadboard for LCD control, robot control, frame grabber, or anything else. In the next step, the dedicated hardware of the application is combined with those parts of the hyperstone develop-

ment board, which are necessary for the target application. An additional small interface connector can be provided to perform fine-tuning of the final product. For such purposes, exactly the same software tools are used as in the first phase. The last step is production. Here, an interface connector can still be used for final tests in combination with a needle tester.

HYPERSTONE SINGLE-CORE RISC/DSP MACRO CELL

In addition to selling complete chips to customers, hyperstone also offers the E1-32X architecture as a single-core RISC/DSP macro cell described in Verilog. It includes all components of the E1-32X except pad logic as shown in Figure 1 and provides all required signals for connecting on-chip peripherals. Upon request, certain function blocks can be removed. It is fully code compatible to the E1-32X stand-alone unit. Simple integration of additional hardware and peripherals is possible and all system development and debugging tools can be used as described above.

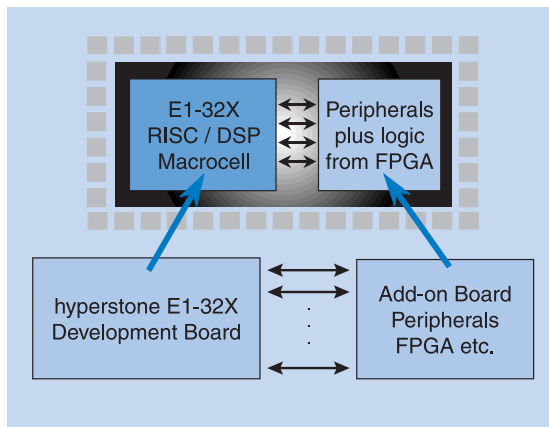


Figure 4: ASIC development using RISC/DSP macrocell

For implementation of the hyperstone RISC/DSP macro cell hyperstone provides extensive design support in the concept phase, for hardware, integration of peripherals, transfer to any CMOS logic process, for software including optimization, drivers, and others.

The development of ASICs using the hyperstone RISC/DSP macro cell is carried out as follows:

The first step is to use the standard hyperstone development board, with the standard hyperstone E1-32X processor. The additional logic, which may be required for the application is implemented in an off-chip FPGA described in Verilog. At this stage, everything can be tested in real-time under real conditions. As a matter of fact, the off-chip logic connects to the on-chip bus interface of the hyperstone RISC/DSP processor.

When everything is fully tested, exactly the same logic in the FPGA can be used for inclusion in the hyperstone RISC/DSP macro cell because the macro cell also contains hyperstone's bus interface. This method reduces the risk of producing chip masks with malfunctions due to logical errors.

With hyperstone's single-core RISC/DSP macro cell the following advantages can be achieved: short design time, fast prototyping, macro cell verification already in

the prototype phase, code compatibility between board level and ASIC level, no software modifications required, use of existing system development tools and debug tools, including real-time kernel.

HYPERSTONE F1-8X SINGLE-CHIP ATA FLASH MEMORY CONTROLLER

An example for using the hyperstone E1-32X RISC/DSP macro cell is the flash memory controller hyperstone F1-8X. It is a single-chip controller for ATA flash memory cards / CompactFlash memory cards. Hyperstone F1-8X is able to support flash memory chips from Samsung, Hitachi, Toshiba, Mitsubishi, AMD, and compatibles.

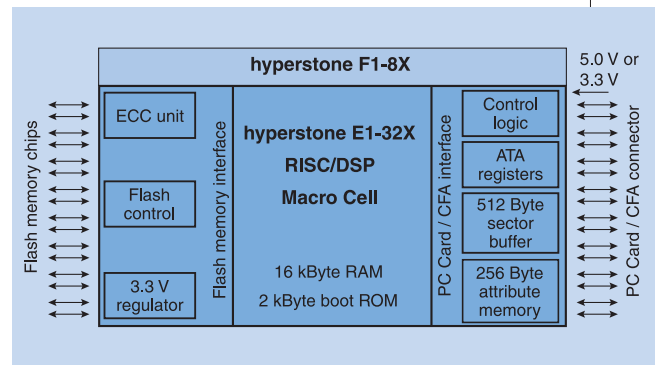


Figure 5: hyperstone F1-8X flash memory controller

The hyperstone F1-8X flash memory controller contains the following function blocks: hyperstone E1-32X RISC/DSP macro cell with 16 kByte RAM and 2 kByte boot ROM, Flash memory interface with an on-chip 3.3V regulator, Flash control logic and logic for error detection and -correction, PC card / CFA interface with a 256 Byte attribute memory for the CIS (card information structure), control logic, ATA registers, and a 512 Byte sector buffer for data interchange with the host system. The same hyperstone F1-8X can operate from a 5V or from a 3.3V source. Up to 20 MBytes / sec data transfer rate to flash memories can be achieved, and up to 16 MBytes / sec to host using true-IDE PIO mode 4.

SUMMARY AND OUTLOOK

It has been shown that hyperstone's unified RISC/DSP processors are based on a full architectural integration of DSP functions into a RISC architecture. Features and specifications have been described, including system development tools and application software. Hyperstone's single-core RISC/DSP macro cell has been introduced including the single-chip controller hyperstone F1-8X for ATA Flash memory cards and CompactFlash cards. The next version of hyperstone RISC/DSP chips will be the E1-32XS with integrated SDRAM interface and 120 MIPS performance. ■

Dr. Matthias Steck is director of marketing and sales at hyperstone electronics. He is also pursuing general business development of the company. Prior to joining hyperstone in 1993, Dr. Steck has been working for two years at the software company SAP. He holds a Ph.D. in electrical engineering.